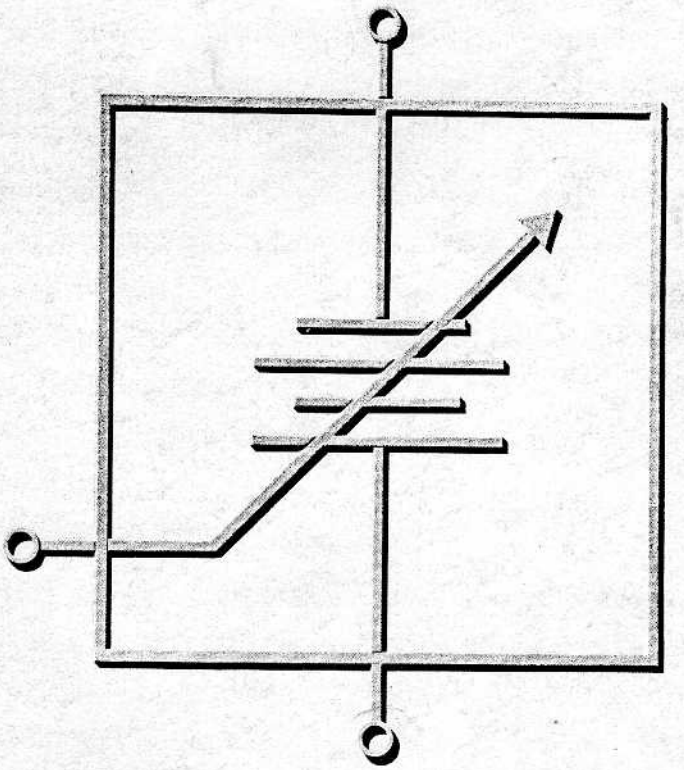
μA723

PRECISION VOLTAGE REGULATOR



Application Notes

FAIRCHILD
SEMICONDUCTOR

TABLE OF CONTENTS

ACKNOWLEDGEMENTS

The authors wish to gratefully acknowledge the contributions of Jim Giles and Murray Siegel for technical assistance, Johan Lund and Larry Stenger for process development and manufacturing of developmental units, Bob Sleeth and Don Lewis for computer programming, data processing, and automatic tester design, and Gail Short and Kay George for typing the manuscripts.

CIRCUIT BUILDING BLOCKS FOR VOLTAGE REGULATORS

by Michael M. Scott

Today the engineer who must decide to buy out or build a power supply is faced with an impressive array of choices. He may buy complete power supplies from many vendors or build a supply using commercially available modules, hybrids or monolithic voltage regulators. He may even decide to design it himself with discrete components and integrated circuit op amps. Voltage regulators consist of basic building blocks shown in Figure 1. The goal is to assemble the blocks to get the typical "ideal" regulator (figure 2).

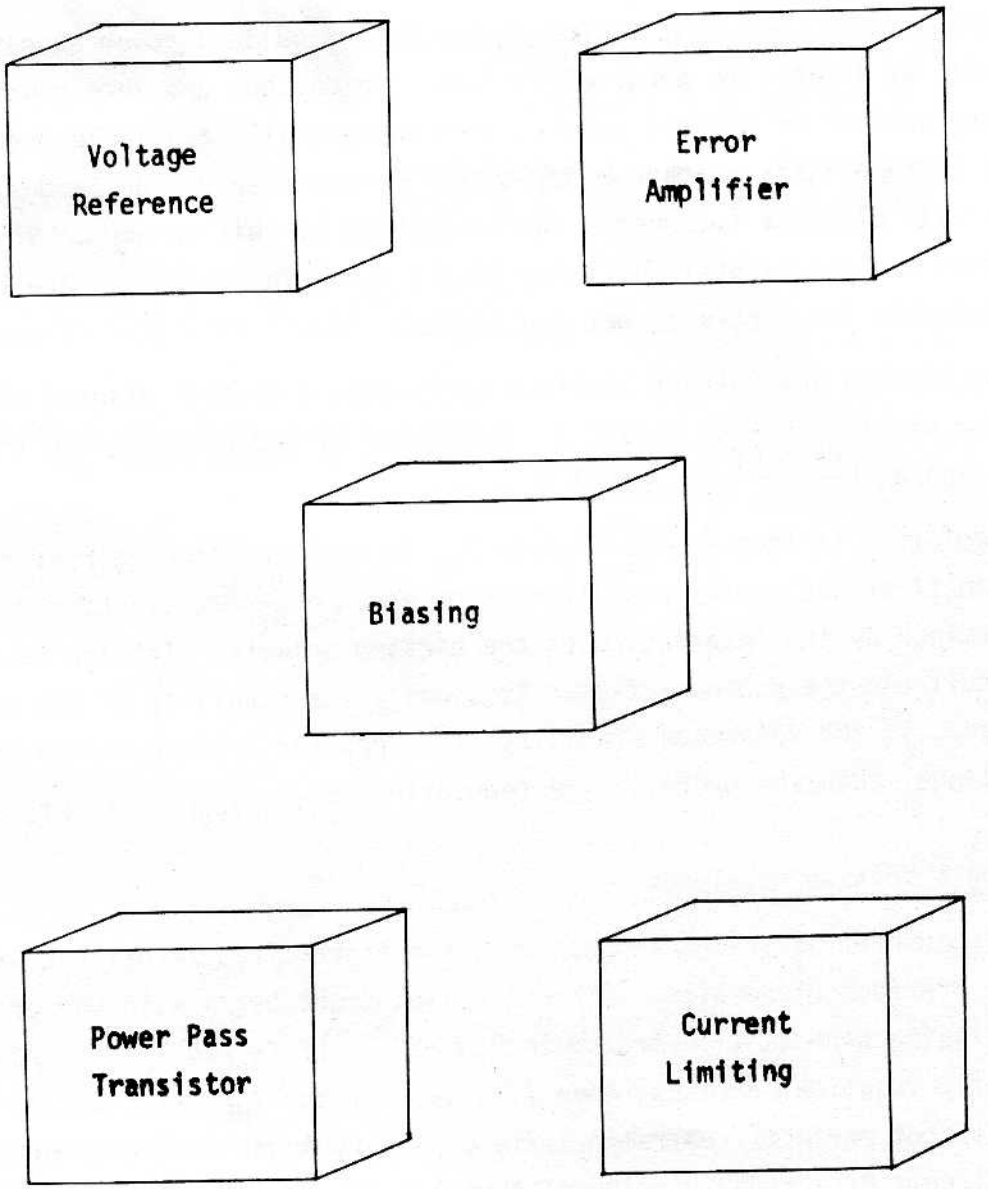
Ignoring biasing and current limiting symbology, a systems diagram of the regulator might look like Figure 3. Resistors R_1 and R_2 establish the output voltage at $[\frac{R_1 + R_2}{R_2} \times V_{REF}]$.

Load Regulation is then $\frac{\Delta A_{VO}/A_{VO}}{1 + \beta A_{VO}}$ where A_{VO} is the open loop gain of the error amplifier and series pass transistor and $\beta = \frac{R_2}{R_1 + R_2}$. Line regulation is determined by the interaction of the biasing networks with the rest of the circuit and the dominant factor is usually the stability of the voltage reference. If the reference stability is ΔV_{REF} for a given change in input line voltage, then the overall line regulation is $\frac{A_{VO}}{1 + \beta A_{VO}} \cdot \Delta V_{REF}$.

Designing a Voltage Regulator

A lot of engineering design and common sense is required to get hardware from the previous discussion. Circuit design might begin with one or more of the biasing schemes illustrated in Figure 4. If T_1 and T_2 in circuit A are exactly identical devices, then $I_1 = I_2$. If the V_{BE} match of the two devices is not perfect, the ratio I_1/I_2 will vary logarithmically with ΔV_{BE}. Circuit B is a PNP version of A with I_1/I_2 varying with the ratio of the collector areas. Temperature stability of these two circuits is poor, but an obvious advantage is their simplicity and minimum parts count.

The use of circuit C is becoming more and more popular today as FET prices decline. The tolerance in I_1 is poor, but it is useful in designing circuits whose current consumption is independent of supply voltage. Without its use, minimum pre-load requirements waste several milliamps in order to



BASIC BUILDING BLOCKS FOR VOLTAGE REGULATORS

FIGURE 1

SIMPLE REGULATOR BLOCK

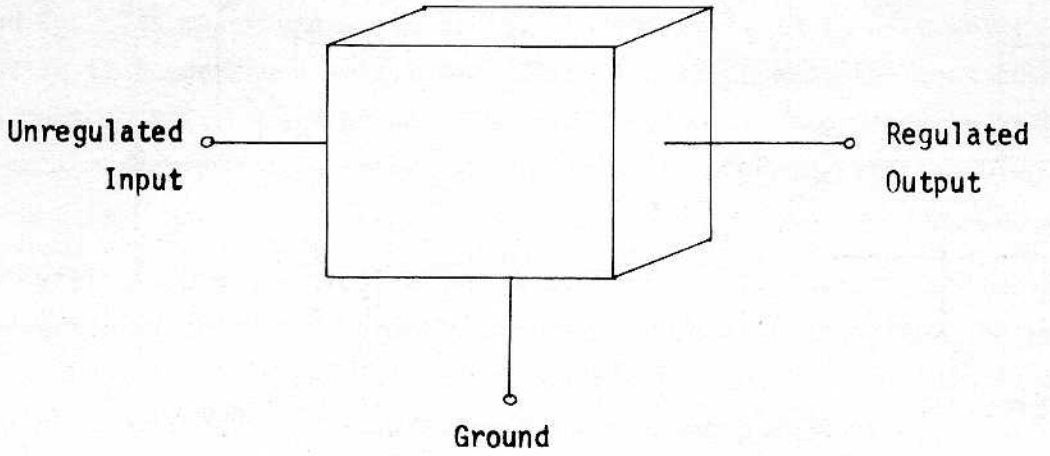


FIGURE 2

REGULATOR BLOCK DIAGRAM

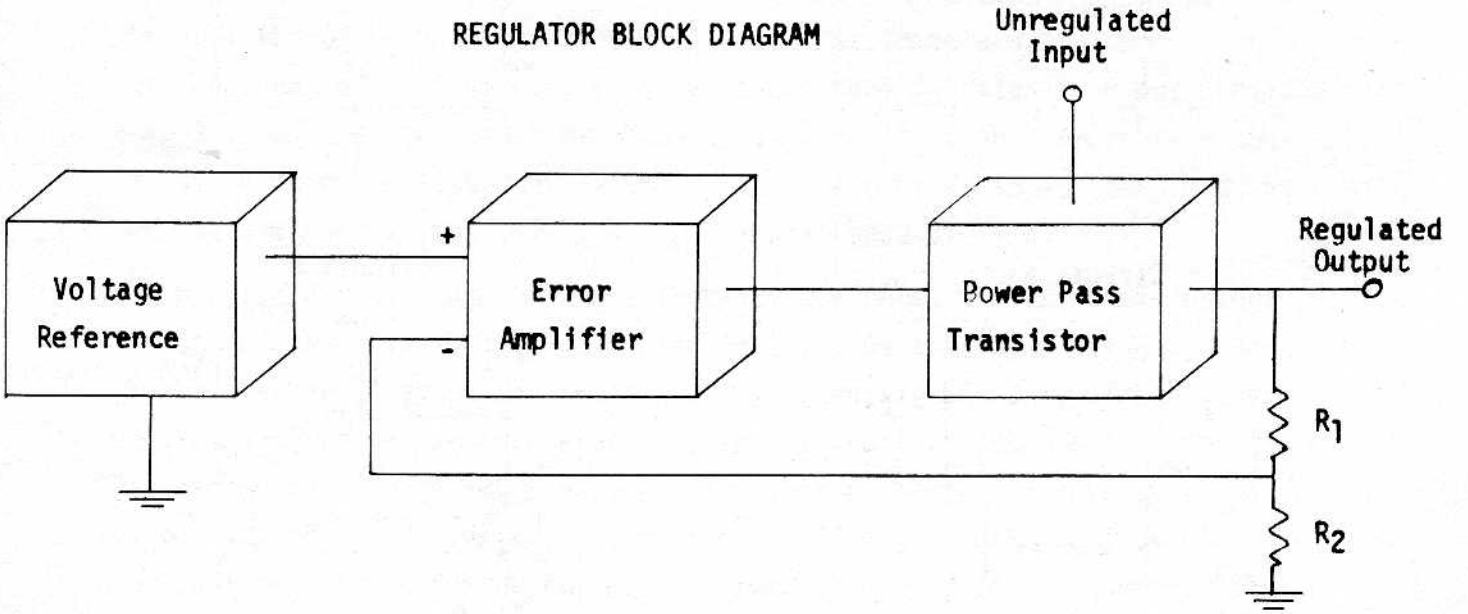
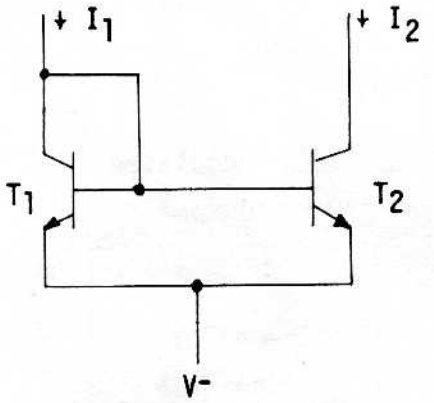
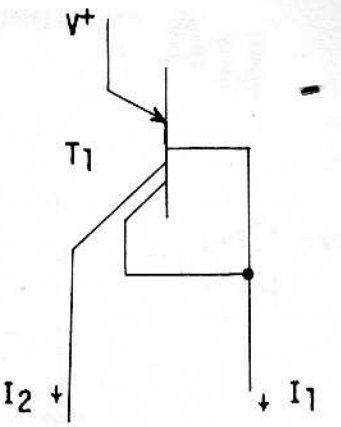


FIGURE 3

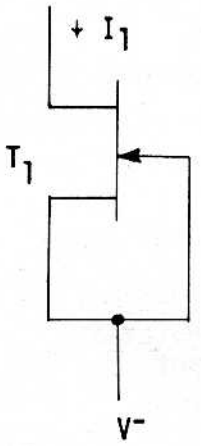
Circuit A



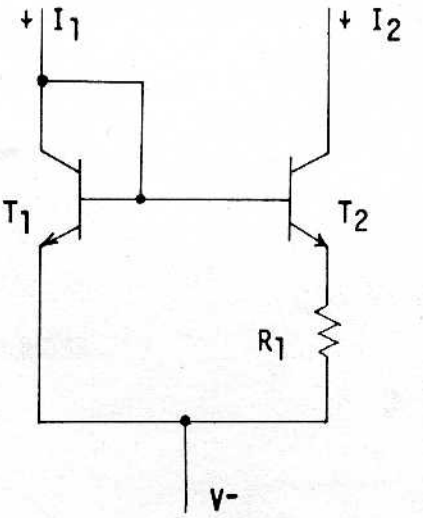
Circuit B



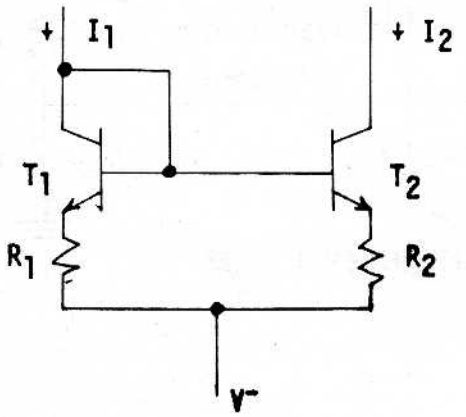
Circuit C



Circuit D



Circuit E



Circuit F

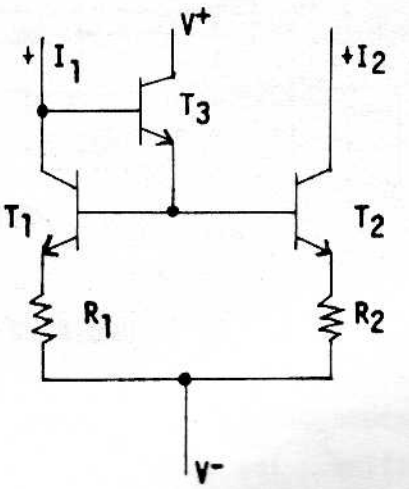


FIGURE 4

BASIC CURRENT SOURCE CONFIGURATIONS

assure start up.

Circuit D is a logarithmic current source and requires close match of T_1 and T_2. Its major use is to achieve ratios of I_1 to I_2 of greater than 5, but it is temperature sensitive. Circuit E is perhaps the most common current source configuration. The I_1/I_2 ratio is determined by R_1/R_2 with good accuracy and temperature stability with only moderate matching of T_1 and T_2.

Circuit F is a Second Generation version of E. It features better matching and tracking because T_3 greatly reduces errors resulting from the non-zero base currents of T_1 and T_2. In monolithic design, this circuit is also useful in establishing accurate and temperature stable integer ratios of I_1 and I_2. To do this, T_2 is made with multiple emitters and multiple emitter resistors with each resistor equal to R_1. This technique maintains equal temperature coefficients for T_1 and T_2 for unequal collector currents.

Figure 5 illustrates several possible voltage references. Circuit G is the simplest. Its line rejection is poor, being the ratio of R_1 to the dynamic impedance of D_1 and it has a very poor temperature coefficient. Line rejection is improved by adding a current source obtaining circuit H. The addition of D_2 and selection of I_1 provides temperature compensation for the zener diode. Circuit I performs the same function as H but provides a V_{REF} lower than the zener breakdown. In circuit I, the temperature compensation is accomplished by selecting the ratio of R_1 to R_2 such that the temperature coefficients of D_2 and D_3 cancel those of T_1 and D_1.

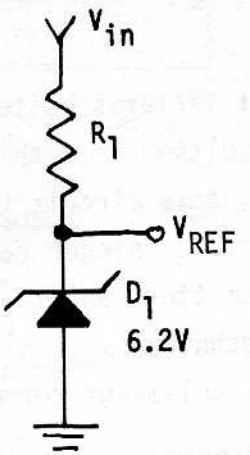
The biggest disadvantage of these voltage references is that their output impedances are relatively high. Circuit J solves this by placing the zener in the feedback loop of an amplifier. Although circuit J is simpler and provides better temperature stability than circuit I, its use in First Generation regulators has been generally avoided because frequency compensation of the amplifier is required. With today's Second Generation technology, low cost monolithic MOS capacitors are readily available and configuration J economically feasible.

The most common error amplifier configurations are shown in Figure 6. The power pass transistor, T_2, and divider resistors have been included for clarity. Usually T_2 is a darlington configuration to provide higher current gain and to prevent loading of the error amplifier. The simplest and most common, circuit K, combines reference and error functions with the emitter

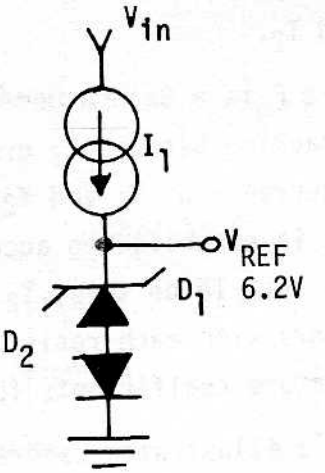
FIGURE 5

BASIC VOLTAGE REFERENCE CONFIGURATIONS

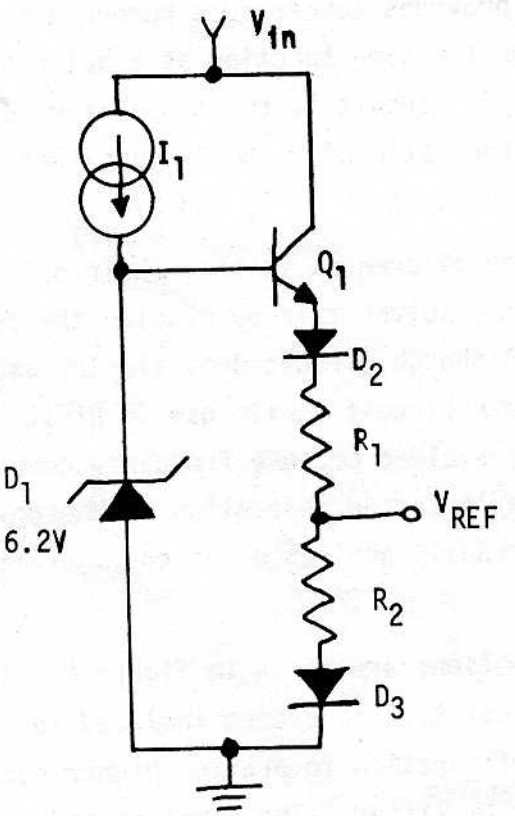
Circuit G



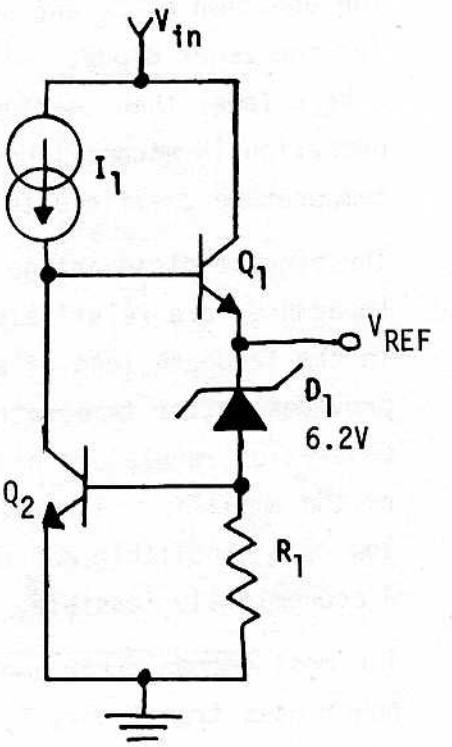
Circuit H



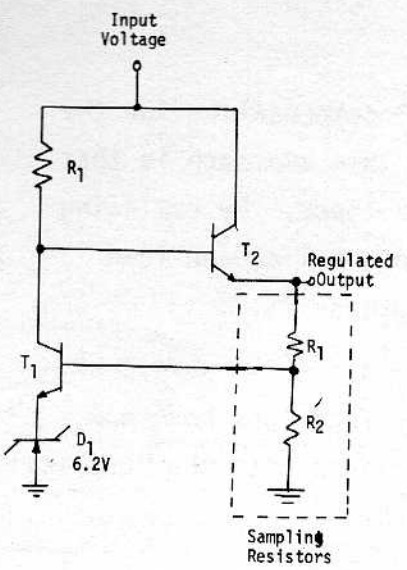
Circuit I



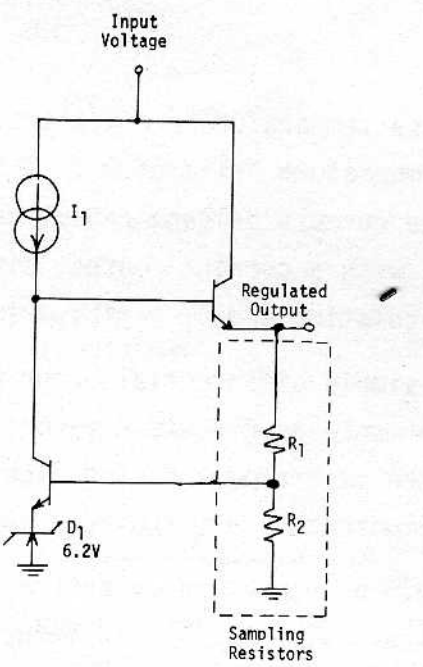
Circuit J



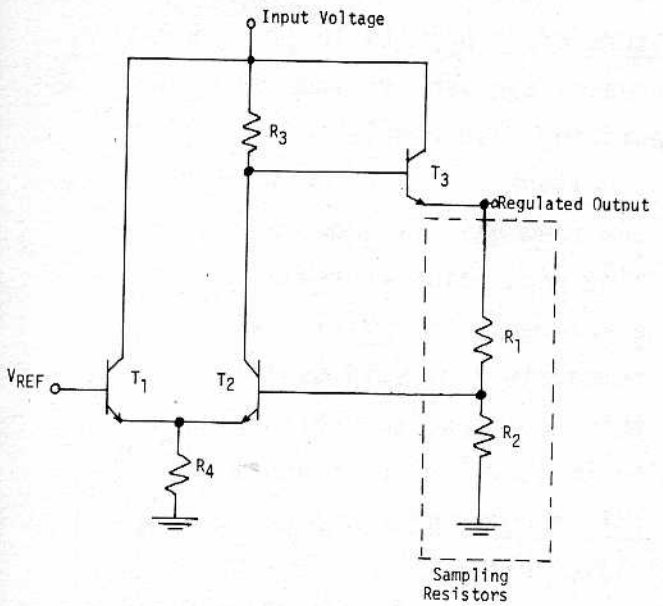
Circuit K



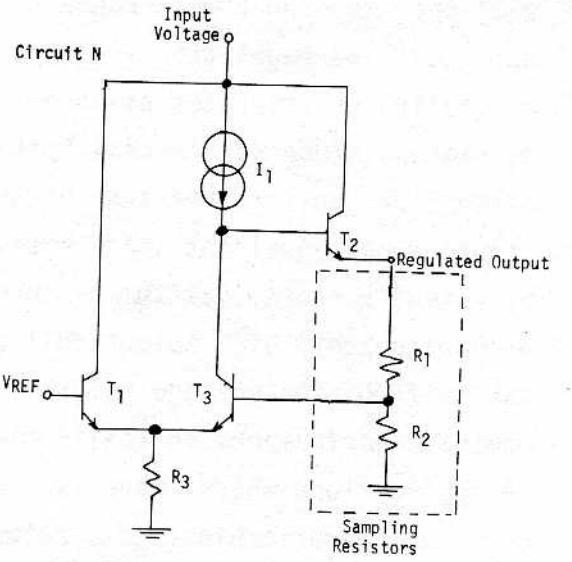
Circuit L



Circuit M



Circuit N



Circuit O

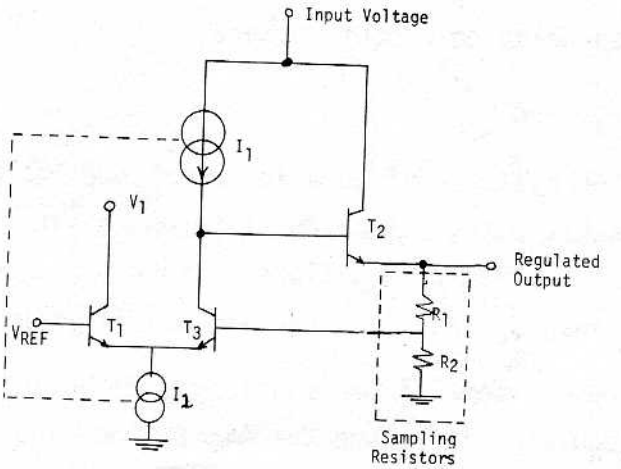


FIGURE 6

base temperature coefficient of T_1 providing partial compensation for the temperature drift of D_1. The major disadvantage of this approach is that the outputs voltage cannot be less than D_1's zener voltage. By replacing R_3 with a current source, circuit L shows improvement in line and load regulation and I_1 may be trimmed to reduce temperature drift.

A simple differential error amp, circuit M, provides about the same performance as circuit K except the reference and error functions have now been separated. Performance improvements may be obtained with the modifications illustrated in circuits N and O.

Before assembling an entire regulator, the following configurations, illustrated in Figures 7 through 9, should be considered. All circuits will operate over a wide range of output voltages. The circuit in Figure 7 has good line regulation and moderate temperature drift but its load regulation deteriorates as output voltage increases because its loop gain decreases. (One can conceal this fact by specifying load regulation in percent per volt rather than percent of output voltage.) The circuit in Figure 8 has excellent load regulation since the loop gain is independent of output voltage. But temperature drift and line regulation increases proportionately with output voltage, since the reference amp multiplies the drift of the voltage reference. Because temperature effects usually dominate performance in realizable circuits, this approach is undesirable in applications where there is a wide variation in load (hence internal dissipation) or ambient temperature. Figure 9 is a compromise between the two previous approaches with resistors dividing either the reference voltage or the output voltage depending on desired output. This configuration has excellent line regulation, temperature stability and excellent to good load regulation, depending on output voltage.

N Voltage Regulators

Using the circuit and system configuration discussed, an engineer could construct approximately 3 X 4 X 3 or 36 different basic voltage regulators (excluding different biasing combinations). Some are already commercially available from various manufacturers and are illustrated in Figure 10.

These circuits represent some of man's attempts to build the ideal three terminal voltage regulator of Figure 2. Since wide ranges of voltages and currents are required in the electronics industry today, most regulators have more than three pins available so that output voltage may be selected

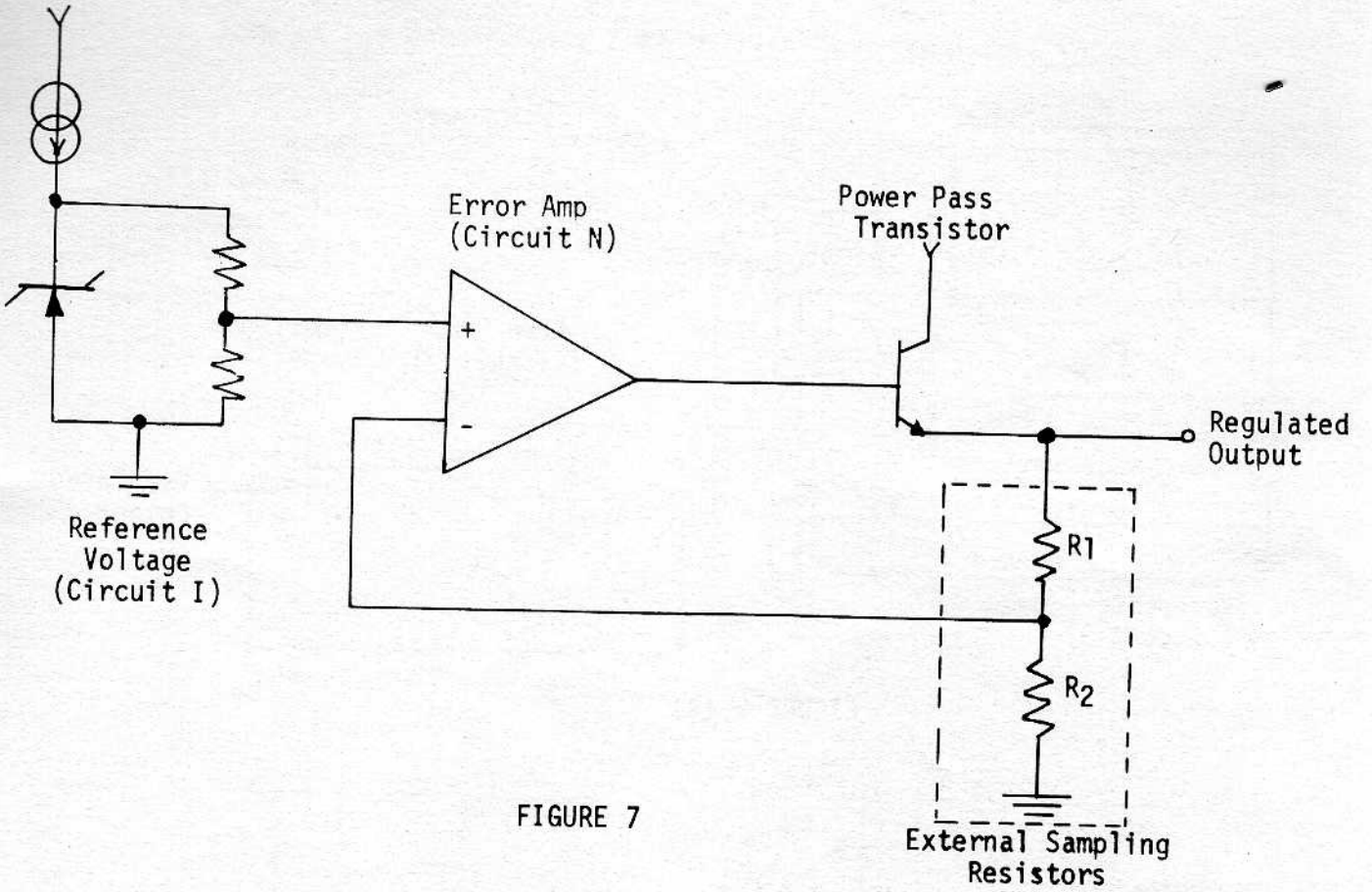


FIGURE 7

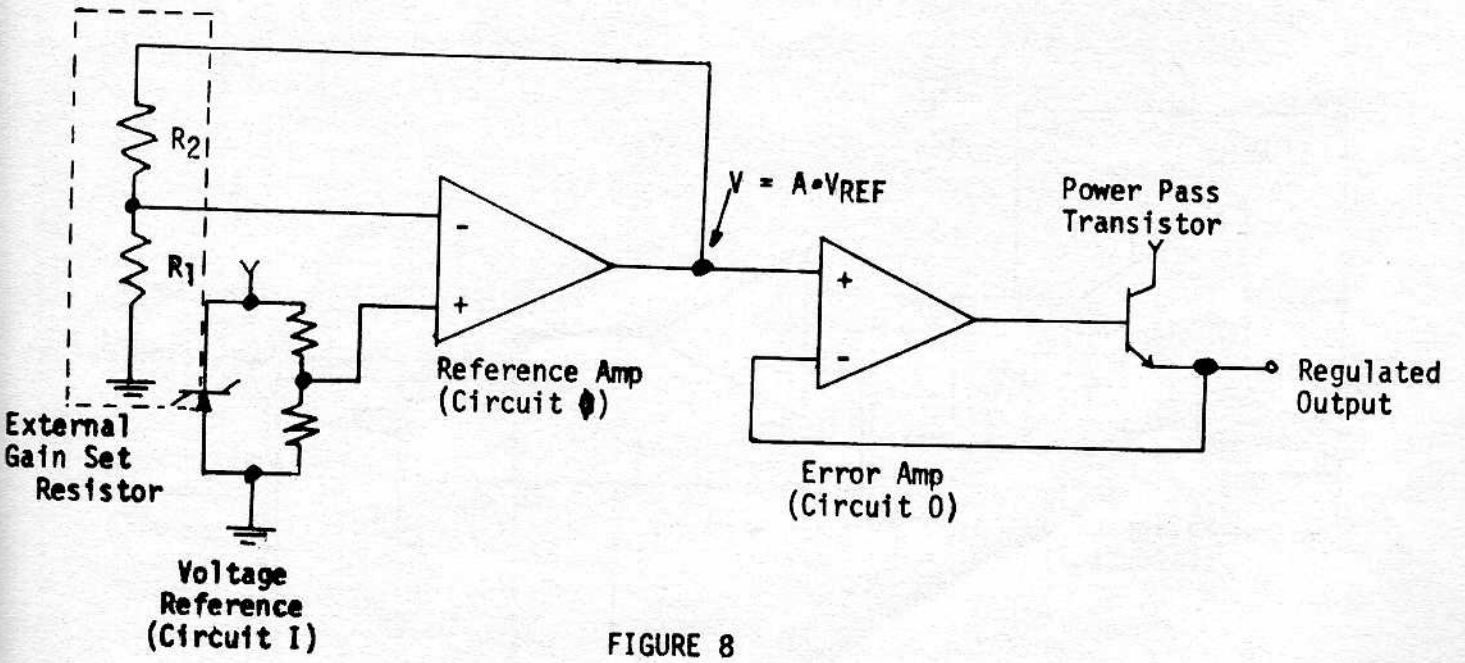


FIGURE 8

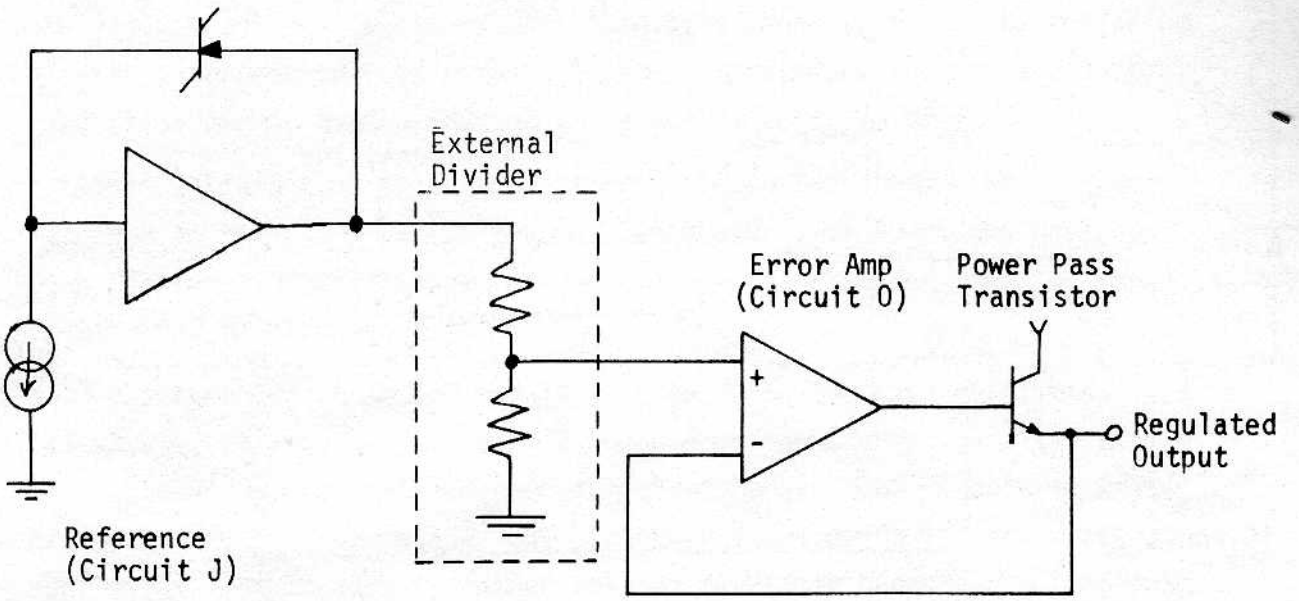


FIGURE 9 (A)

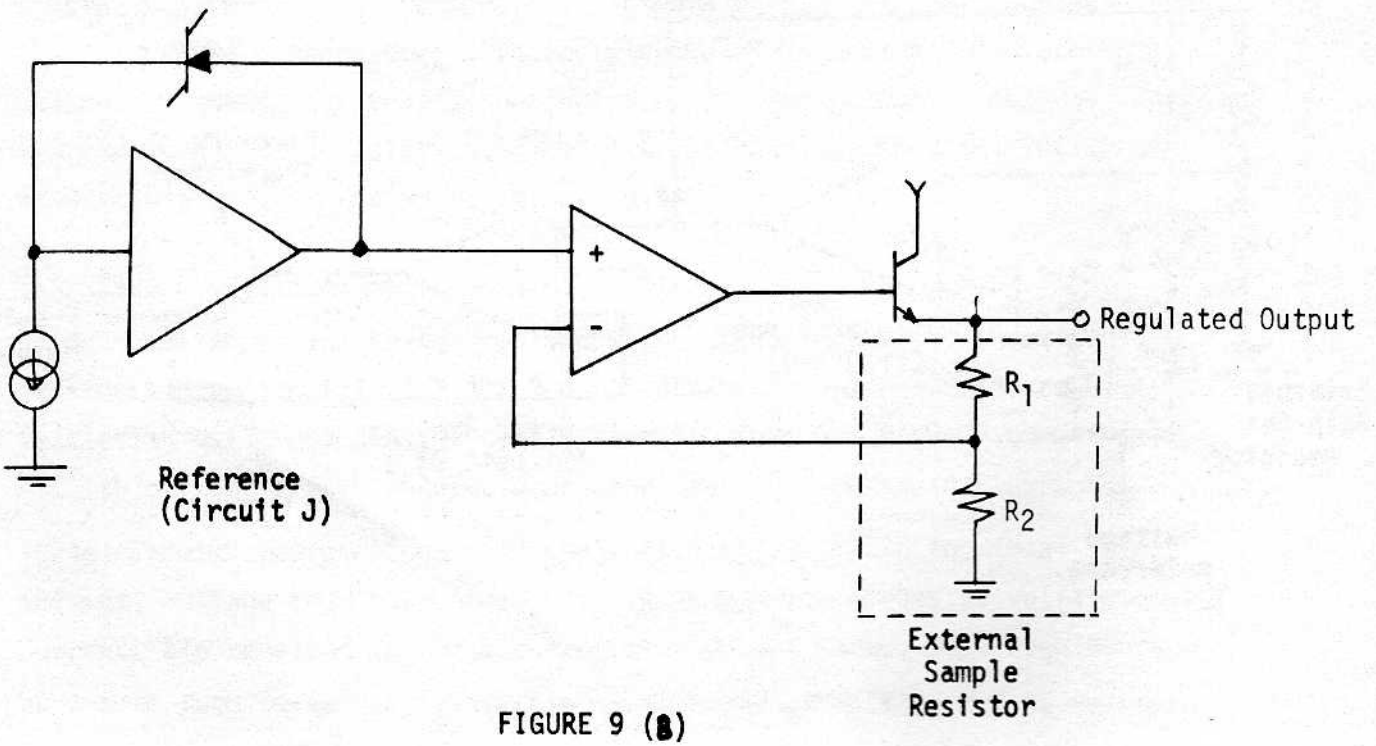
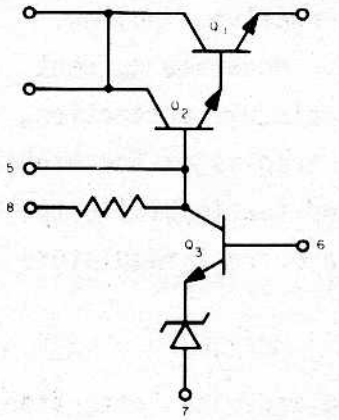


FIGURE 9 (B)

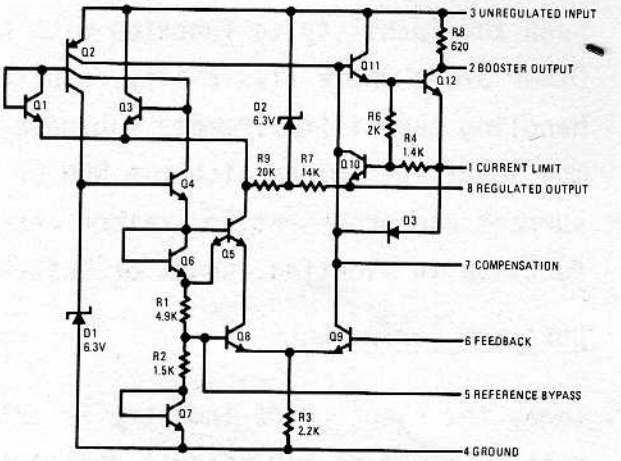
FIGURE 10

Some of the Commercially Available Voltage Regulators

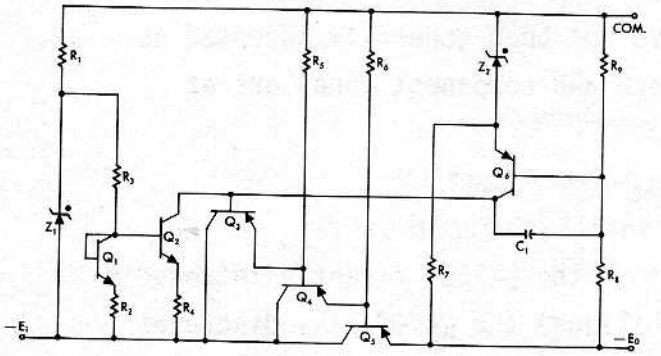
(A)



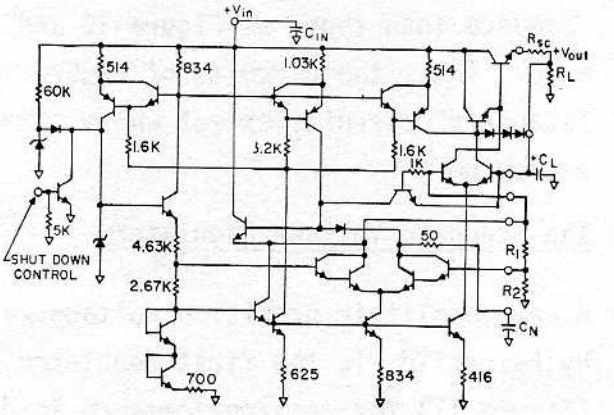
(B)



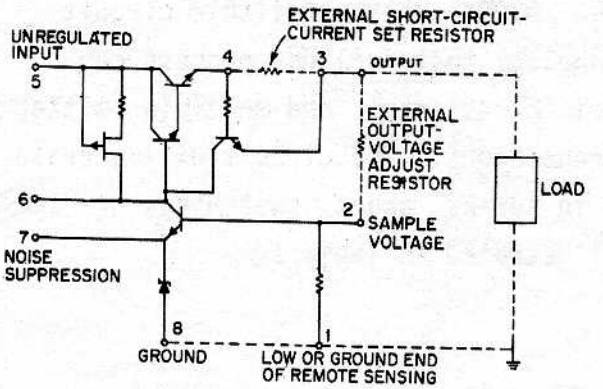
(C)



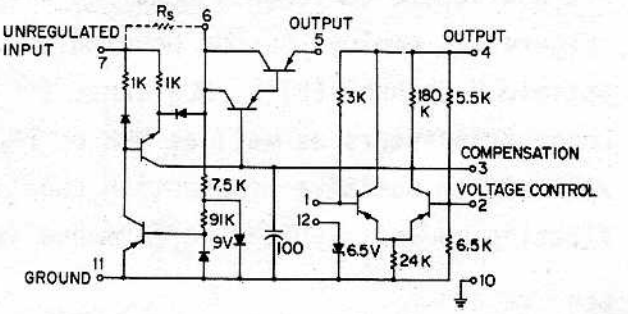
(D)



(E)



(F)



externally. It is unfortunate, therefore, that in minimizing pin count, many of the circuits in Figure 10 are unnecessarily limited in scope of application for want of an extra pin or two. The major limitation has been the inability to function with both positive and negative supplies. Other areas where flexibility is often compromised are: Moderate current handling capability, remote shutdown capability, short circuit protection, the inability to use either a NPN or PNP external pass transistor for higher current and power ratings rather than only one type, and the inability to function in floating, shunt or switching modes, or as a current regulator.

Cost and Performance

Today the electronics industry is extremely competitive and close attention must be given in any circuit design to cost/performance ratio in order to remain competitive in tomorrow's market. This is true today even in Military electronics. It is significant, therefore, that a regulator built with discrete parts and a monolithic op amp (Figure 11) has equal or better performance than those of Figure 10 and is lower in cost by a factor of two or more. Thus, the circuits of Figure 10 have not been generally accepted as "standard" circuits except where board space and component count are at a premium.

The Standard Voltage Regulator

A new monolithic precision voltage regulator, the μA723, recently introduced by Fairchild, is the first regulator to challange the μA709 plus discretes (Figure 11) for cost/performance leadership to become the industry's standard voltage regulator. First and foremost, the μA723 is low cost, being industrially priced about 35% lower than the μA709C, not including the cost of extra discrete components required with the μA709. This monolithic circuit (Figure 12) employs Second Generation technology that includes process compatible N-Channel FET's, MOS capacitors, pinch resistors, and multiple emitter power transistors as well as NPN or PNP transistors. The circuit will operate with either positive or negative supplies in series, shunt, switching, or floating modes. Typical performance is illustrated in Table I.

Conclusion

Various circuit and system configurations for voltage regulators have been discussed. Advantages and disadvantages of existing designs have been

contrasted and a new monolithic regulator, the μA723, which overcomes most of the objections to existing circuits, presented.

TABLE I

μA723

Typical Performance

Line Regulation (ΔV_{in} = 30V)	.02%V_{out}
Load Regulation (ΔI_L = 50mA)	.03%V_{out}
Ripple Reduction	74dB
Temperature Stability	.002%/°C
Output Voltage Range	2 to 37 Volts
Output Current Range	0 to 150mA

FIGURE 11

Voltage Regulator using μA709

Operational Amplifier and Discrete Parts

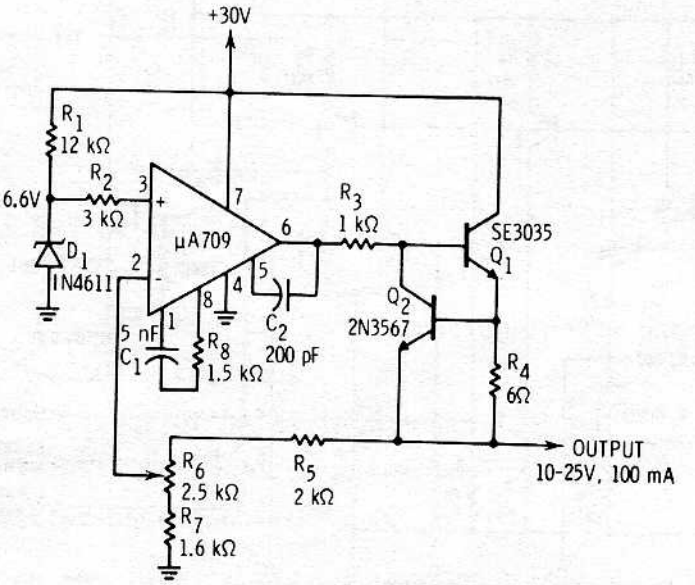
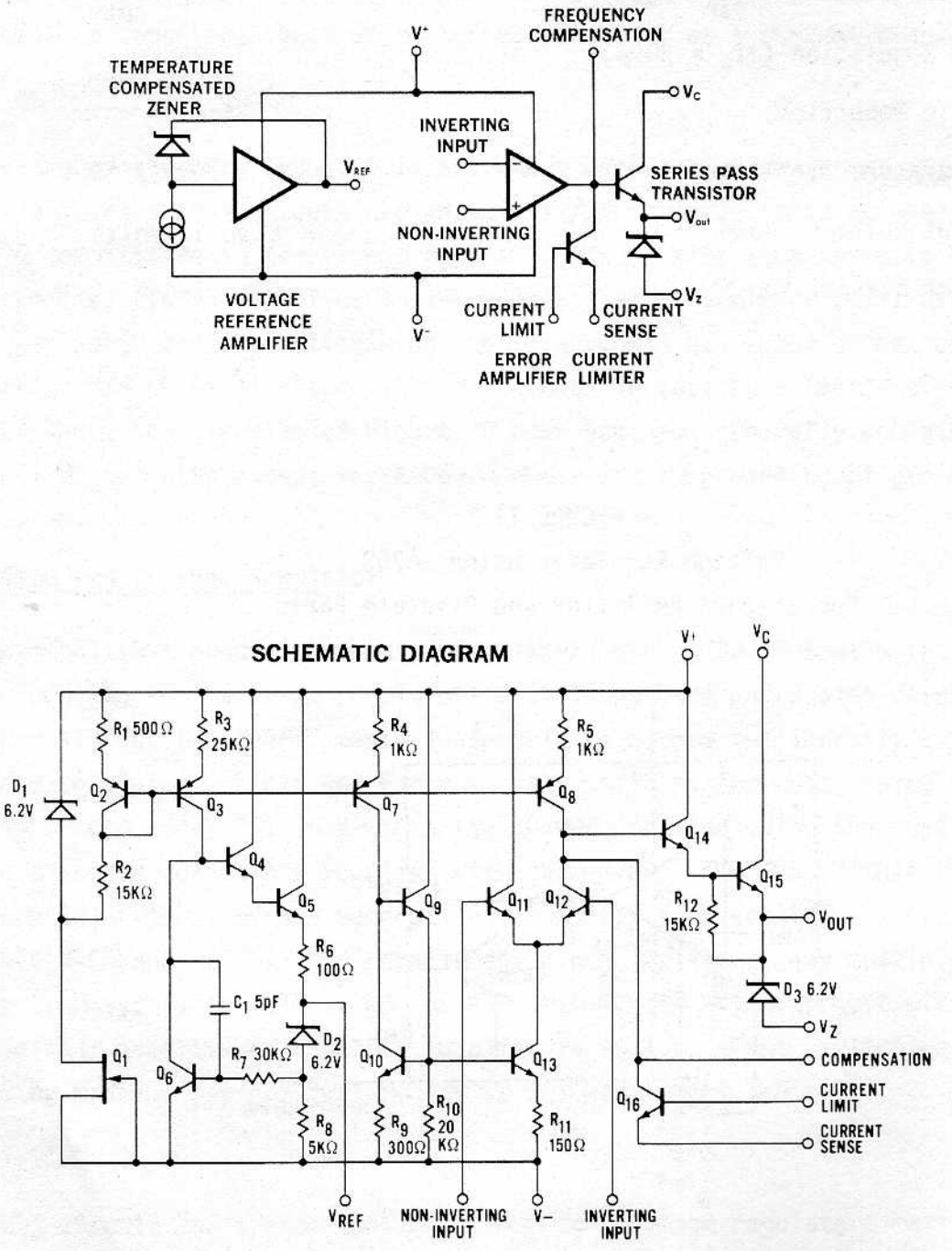


FIGURE 12

FAIRCHILD μA723 PRECISION VOLTAGE REGULATOR



A NEW VERSATILE PRECISION VOLTAGE REGULATOR

BY J. Darryl Lieux

Introduction

Even though in recent months several monolithic and hybrid voltage regulators have been introduced, each of these has had several disadvantages. These include: Low accuracy, low output current, need for expensive pass elements, and inability to operate from high voltage or negative supplies. This paper describes a new circuit which overcomes most of these disadvantages. In addition, units are competitively priced with discrete designs.

Circuit Description

The basic voltage reference schematic is given in Figure 1. The basic reference element is the zener diode D_1 which has a typical breakdown voltage of 6.2 volts at 100μA and a temperature coefficient of 2.4mV/°C. Resistor R_1 is used to bias D_1 to its operating current.

The basic equation for the V_{BE} of Q_1 is given in equation (1):

$$V_{BE} = \frac{kT}{q} \ln \frac{I_C Q_B}{q D_p n_i^2 A_E} \qquad \text{OR}$$

$$V_{BE} = \frac{kT}{q} \ln \frac{Q_B}{q D_p n_i^2 A_E} + \frac{kT}{q} \ln I_C \qquad (1)$$

where:

$\frac{kT}{q}$ = 25.6mV at 25°C

Q_B = un-ionized impurity concentration in the base

q = 1.6×10^{-19} coulombs

D_p = diffusivity of holes in the base

n_i = intrinsic carrier concentration

A_E = emitter-base junction area

The first term on the left is independent of collector current and will have the same temperature coefficient regardless of the collector current. The

FIGURE 1

Simplified Voltage Reference Schematic

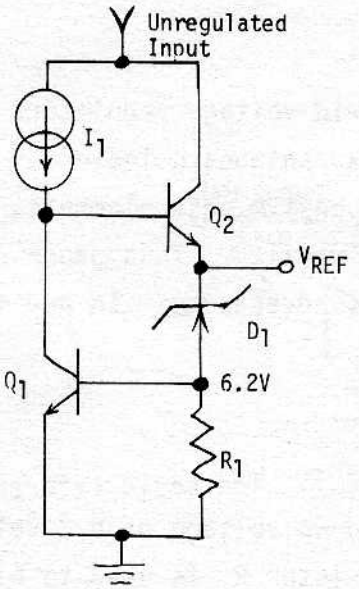


FIGURE 2

Simplified Error Amplifier Schematic

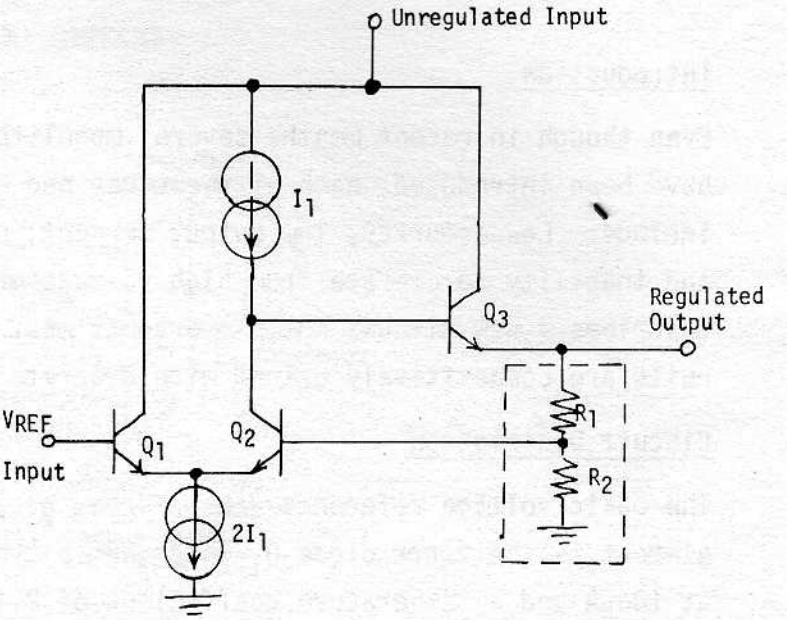
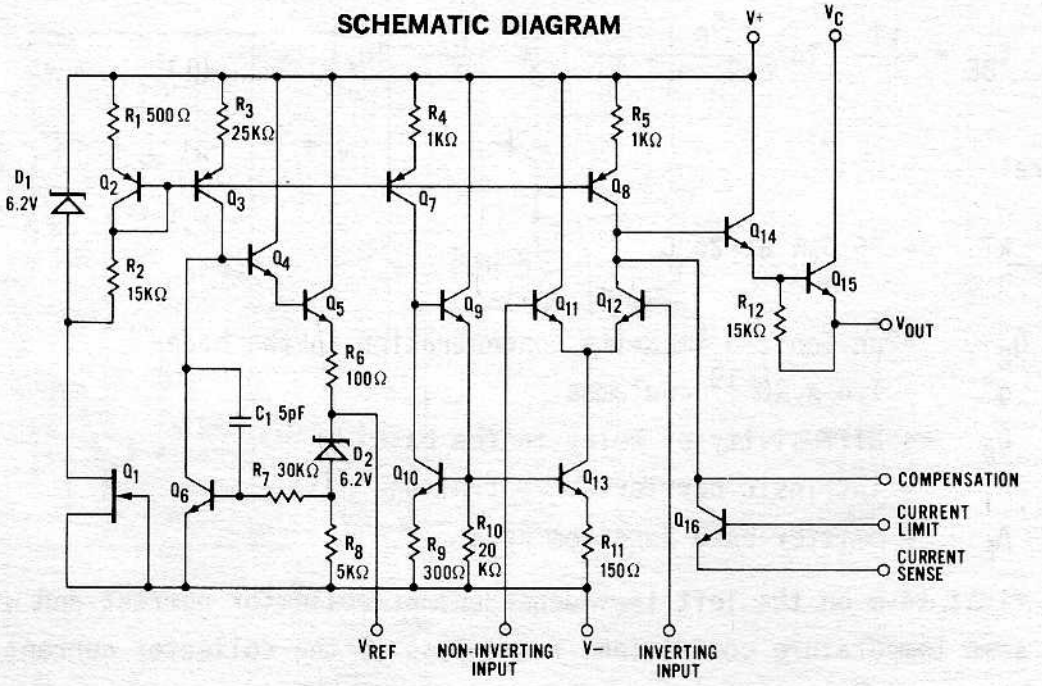


FIGURE 3



second term depends on the collector current and causes the V_{BE} temperature coefficient dependence on collector current. This dependence is 0.2mV/°C for each decade increase in collector current. Thus, collector current of Q_1 can be varied to match the temperature coefficient of D_1 by varying the current source I_1, setting the net temperature coefficient at zero. Variations in I_1 change only the V_{BE} of Q_1 and not the breakdown voltage of D_1 with resulting low variation in the value of V_{REF}. Transistor Q_2 supplies the current for D_1, R_1, and any external loads.

Figure 2 shows the simplified schematic for the error amplifier section. Transistors Q_1 and Q_2 form a differential pair driven by the current source, $2I_1$. The voltage on the V_{REF} input will be equal to the voltage between R_1 and R_2 and the output voltage is:

$$E_0 = \left(\frac{R_2 + R_1}{R_2}\right) V_{REF} \qquad (2)$$

Knowing V_{REF}, R_1 and R_2 can be selected for the desired output voltage.

Transistor Q_3 is used as a buffer to prevent loading on Q_2. The gain, K_V, from the base of Q_2 to the output is:

$$K_V = q \frac{I_1 R_p}{2 kT} \qquad (3)$$

where R_p is the effective loading on the collector of Q_2. If R_p is very large, the gain can be made very high. This is done by using a PNP current source as a collector load for Q_2. In this way, a single stage can provide adequate voltage gain for the error amplifier function. Compensation is also greatly simplified because only one stage need be compensated.

Figure 3 illustrates the complete schematic of the μA723 Voltage Regulator. The biasing network for the PNP current sources Q_3, Q_7, and Q_8 is comprised of transistors Q_1 and Q_2, diode D_1, and resistors R_1 and R_2. Transistor Q_1 is an N-Channel FET made with technology compatible with the production of normal integrated circuit components. The use of a FET has two advantages: First, the line regulation is greatly improved because the current drawn by Q_1 is independent of power supply variations and secondly, the power dissipation is minimized because the current drawn does not increase appreciably at large supply voltages. Diode D_1 is used to regulate the bias network voltage and provides a very well-regulated voltage at the base of Q_2 with respect to V+.

Transistors Q_3, Q_7, and Q_8 form the current sources discussed previously. The normal method of biasing these current sources is to either use a diode-connected transistor with the same current as shown in Figure 4, or to use a logarithmic relationship as shown in Figure 5. However, for this design, very high output impedance is required to provide high line rejection and increase the gain of the error amplifier. Referring again to equation (1), a decrease in Q_B will produce an increase in I_C for constant V_{BE}. Since an increase in the collector-to-emitter voltage of the transistor widens the depletion region and lowers Q_B, I_C increases with an increase in collector-to-emitter voltage giving a lower output impedance. If, however, the configuration shown in Figure 6 is used, the current is:

$$I_{C_2} = \frac{V_B - V_{BE_3}}{R_2} \qquad (4)$$

Now a change in V_{BE} has only a small effect on the voltage across R_2 and the collector current is constant with changes in collector-to-emitter voltage providing very high output impedance.

To achieve low output impedance, transistor Q_2 in Figure 1 has been replaced in Figure 3 with a darlington pair Q4 and Q_5, resistor R_7 and capacitor C_1. The MOS capacitor is included on the chip to eliminate the need for any external compensation of the voltage reference loop.

The power pass transistor, Q_{15}, is actually a multiple device with individual emitter resistors to prevent "current-hogging", increase safe operating area thus preventing secondary breakdown, and providing up to 150 mA output current.

Performance Characteristics

The basic regulator circuit is given in Figure 7 and the typical performance attained in Table I. Resistors R_1 and R_2 divide down the reference output, V_{REF}, to the desired output voltage value and is supplied the non-inverting input of the error amplifier. The error amplifier is connected in a voltage-follower configuration. Capacitor C_1 is used to roll off the error amplifier and provide frequency compensation. Resistor R_3 isolates C_1 from the output and balances the input divider. Capacitor C_{REF} may be used to reduce output noise and ripple. Component values given in Figure 7 were used when taking data presented in this section unless otherwise noted.

Performance is further illustrated in Figures 8 through 17. Load regulation (Figure 8) is lower at -55°C because of the decrease in beta of Q_{11} and Q_{12}

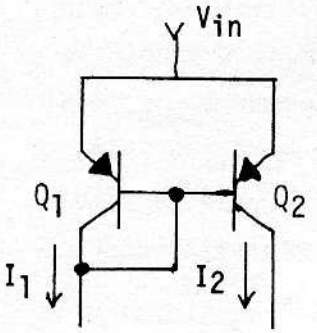


FIGURE 4
DCT Current Source

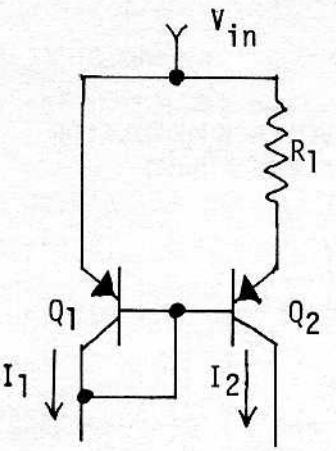


FIGURE 5
Logarithmic Current Source

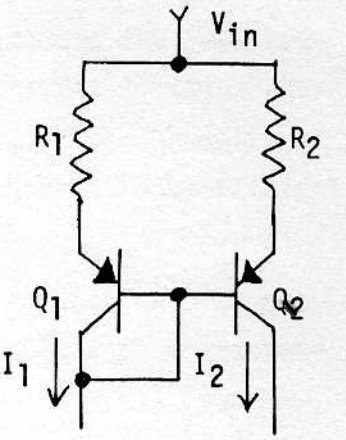


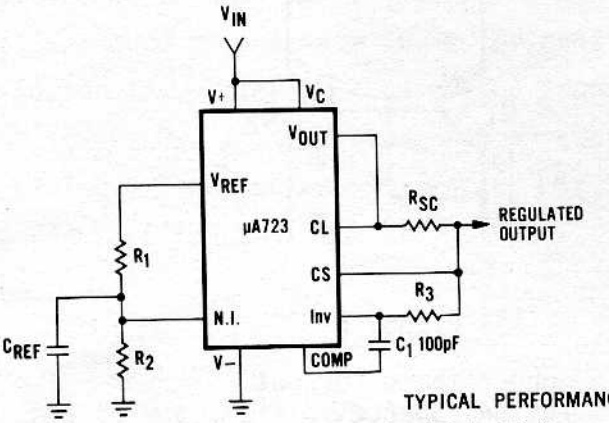
FIGURE 6
High Output Impedance Current Source

TABLE I

Line Regulation (V_{in} = +12V to V_{in} = +15V)	0.01% V_{out}
Load Regulation (I_L = 1mA to I_L = 50mA)	0.02% V_{out}
Ripple Rejection	74dB
Temperature Coefficient of Output Voltage	.002%/°C
Reference Voltage	7.15V
Output Noise Voltage (f = 100Hz to 10KHz, C_{REF} = 0)	20μV_{RMS}
Long Term Stability	0.1%/1000 hrs.
Standby Current Drain (V_{in} = 30V)	2.5mA
Output Voltage Range	2 to 37 Volts
Output Current Range	0 to 150mA

FIGURE 7

BASIC LOW VOLTAGE REGULATOR
(V_{out} = 2 to 7 Volts)



TYPICAL PERFORMANCE

Regulated Output Voltage	5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Note: $R_3 = \frac{R_1 R_2}{R_1+R_2}$ for minimum temperature drift.

FIGURE 8

LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING

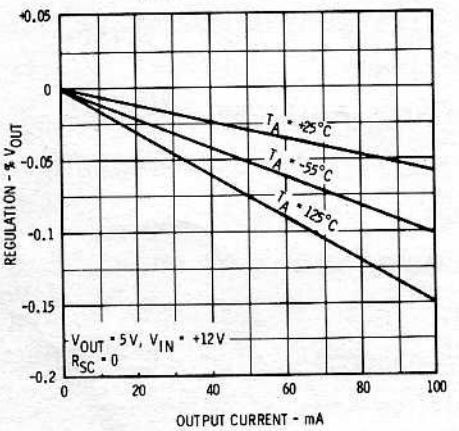
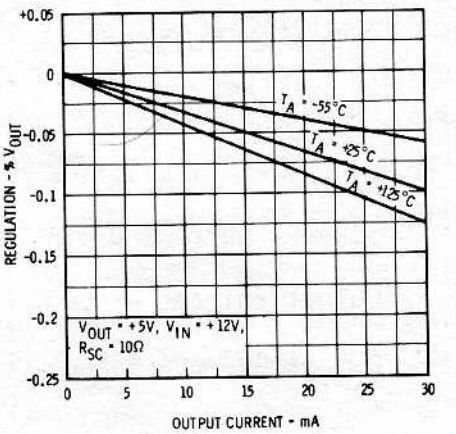


FIGURE 9

LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



and lower at +125°C because the output impedance of Q_{12} decreases at high temperatures decreasing the error amplifier loop gain. This is further illustrated in Figure 9 where the additional voltage drop across R_{SC} causes the load regulation to improve at -55°C and degrade at +125°C. The current limiting characteristics vs. temperature are illustrated in Figure 10 and 11. The current limit value, since it depends on the V_{BE} of Q_{12}, has a temperature coefficient of approximately -0.3%/°C.

Figures 12 and 13 illustrate line and load regulation as a function of input-output voltage differential and Figure 14 illustrates the pinchoff characteristics of Q_1. Standby current is lowest at 125°C reducing internal power dissipation. Figures 15, 16, and 17 show frequency response of the regulator.

Applications

Besides the basic regulator circuit given in Figure 7, the μA723 may be used in numerous other configurations, a few of which are presented here. All circuits shown here are for the TO-5 type package. The circuit shown in Figure 18 is used for output voltages greater than 7V. For optimum temperature tracking, a resistor equal to the parallel combination of R_1 and R_2 should be added between the V_{REF} and non-inverting terminals. This resistor should also be added if a bypass capacitor from the non-inverting input to ground is used to reduce noise and ripple since the output impedance of the V_{REF} terminal is only 1Ω.

A circuit increasing the maximum output current is shown in Figure 19. The values of R_1 and R_2 shown will give approximately 5 volts out. To frequency compensate the additional phase shift provided by Q_1, resistor R_3 has been added, and C_1 has been increased to 510 pF. Resistor R_5 is selected for current limiting at approximately 5 amps.

An alternate to Figure 19 is shown in Figure 20. This circuit uses PNP pass element, Q_1. Resistor R_2 is used to reduce the loop gain and avoid frequency stability problems.

One of the unique features of the μA723 Voltage Regulator is the ability to operate under "floating" conditions. This is possible because both input terminals of the error amplifier are brought out for connection externally. This enables the μA723 to provide not only large positive regulated voltages,

FIGURE 10

CURRENT LIMITING CHARACTERISTICS

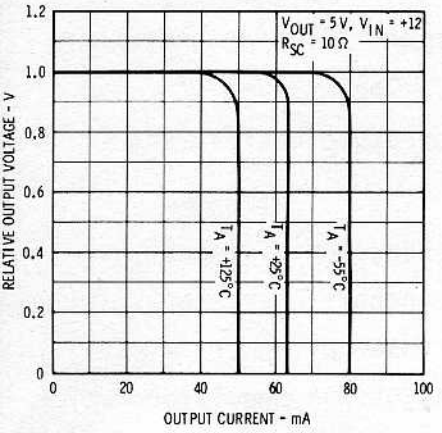


FIGURE 11

CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE

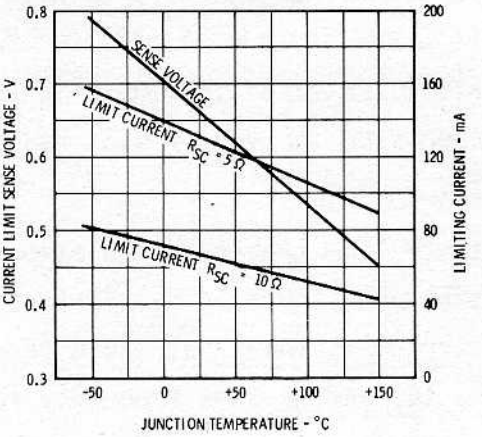


FIGURE 12

LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

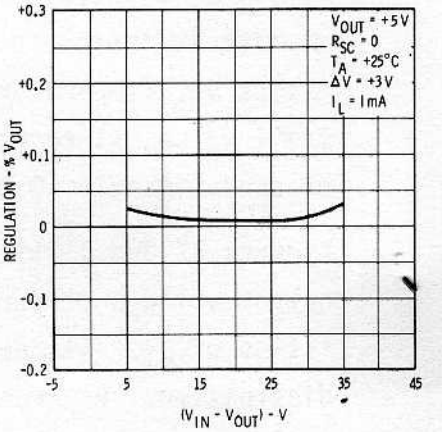


FIGURE 13

LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

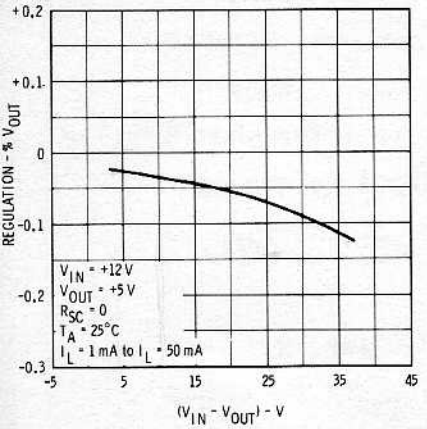


FIGURE 14

STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

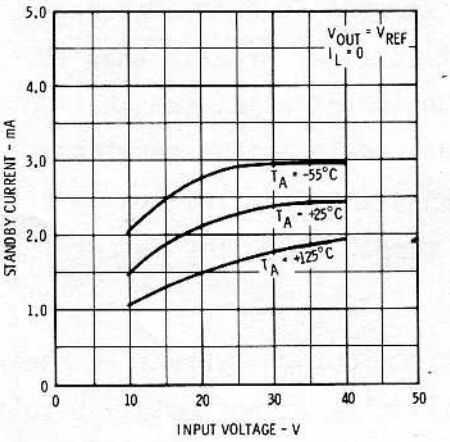


FIGURE 15

LINE TRANSIENT RESPONSE

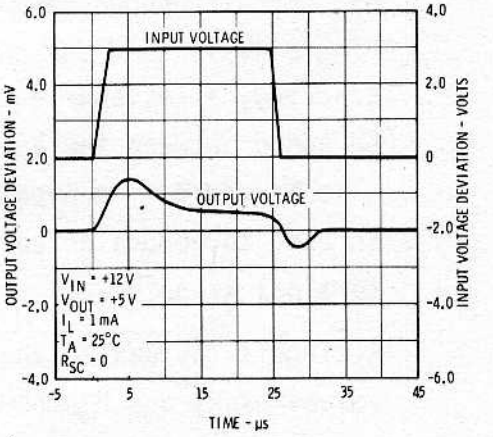


FIGURE 16

LOAD TRANSIENT RESPONSE

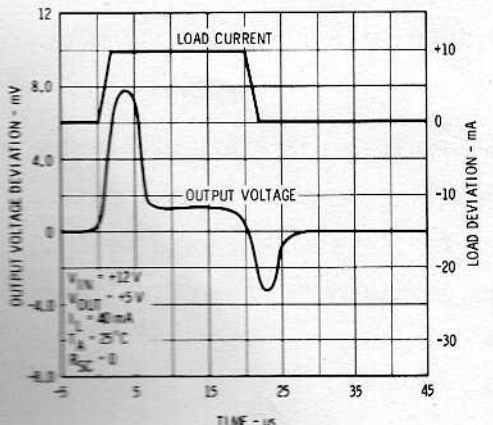


FIGURE 17

OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

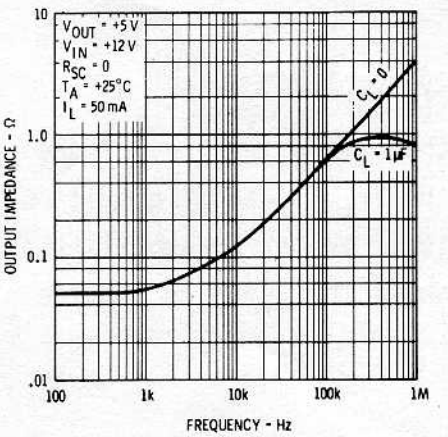
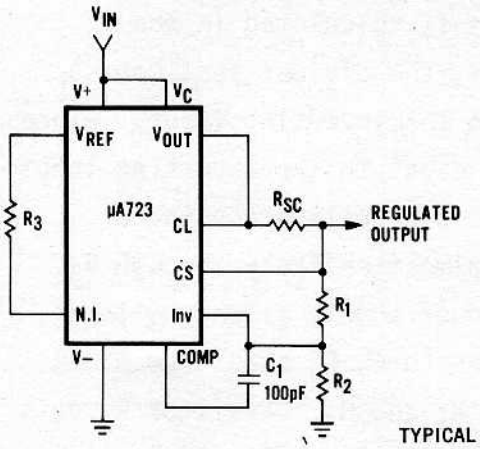


FIGURE 18

BASIC HIGH VOLTAGE REGULATOR
(V_{out} = 7 to 37 Volts)



TYPICAL PERFORMANCE

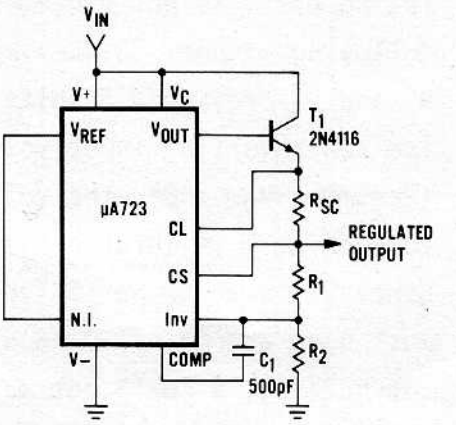
Regulated Output Voltage	15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5 mV
Load Regulation (ΔI_L=50 mA)	4.5 mV

Note: $R_3 = \frac{R_1 \cdot R_2}{R_1 + R_2}$ for minimum temperature drift.

R_3 may be eliminated for minimum component count.

FIGURE 19

POSITIVE VOLTAGE REGULATOR
(External NPN Pass Transistor)

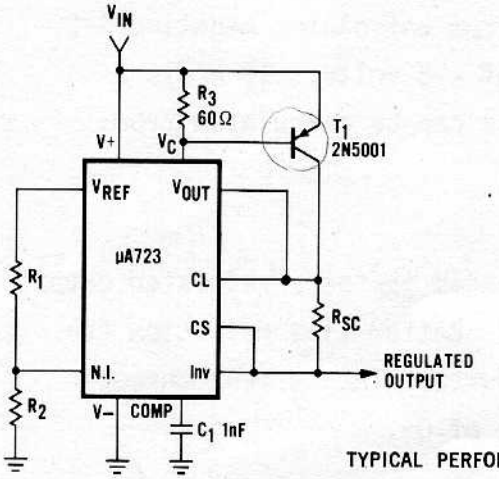


TYPICAL PERFORMANCE

Regulated Output Voltage	+15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5 mV
Load Regulation (ΔI_L = 1 A)	15 mV

FIGURE 20

POSITIVE VOLTAGE REGULATOR
(External PNP Pass Transistor)

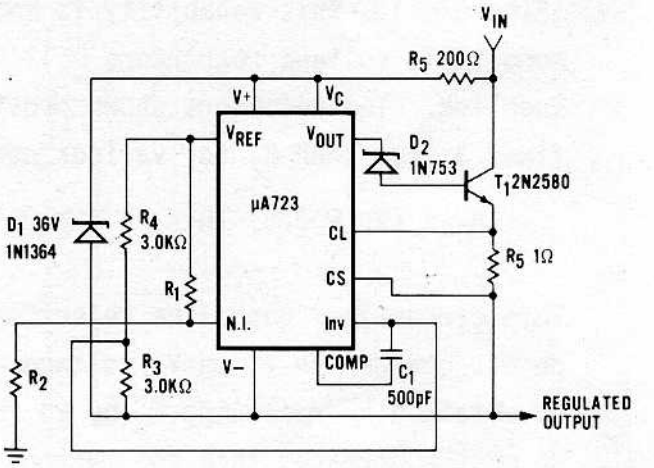


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L = 1 A)	5 mV

FIGURE 21

POSITIVE FLOATING REGULATOR



TYPICAL PERFORMANCE

Regulated Output Voltage	+50 V
Line Regulation (ΔV_{IN} = 20 V)	15 mV
Load Regulation (ΔI_L = 50 mA)	20 mV

but also negative voltage outputs. In addition, an input voltage beyond the absolute maximum rating of the voltage regulator may be regulated down to a low output voltage such as 5 volts using this configuration. A circuit employing floating operation to obtain +50 volts output is shown in Figure 21. The input voltage for this configuration may be from 65 to 100 volts if the voltage rating of T_1 is not exceeded. The output voltage is calculated in the following manner. Since V_{REF} is approximately 7V, the divider resistors R_3 and R_4 provide 3.5 volts with respect to V^- to the inverting input. Since the non-inverting input voltage is approximately equal to the inverting input (assuming $V_{OS} = 0$), the voltage drop across R_1 is 3.5 volts producing a current of 1 mA through R_1. This current flows almost entirely through R_3. Since V^- is to be at +50 volts with respect to power supply ground R_3 then must have a drop of 50 +3.5 volts across it. Therefore, R_2 should be 53.5K. For nulling, a small pot may be inserted between R_1 and R_2. Resistor R_6 sets the current limiting value at approximately 600mA. Resistor R_5 and D_1 limit the voltage across the µA723 to 36 volts when the output is shorted to ground. Diode D_2 used to shift the V_{OUT} terminal of the µA723 up to provide sufficient operating voltage to Q_{12}. D_2 can be eliminated when using the DIP package by using the V_Z terminal instead of the V_{OUT} terminal. The standby current of the µA723 flows into the output load as does the current through R_3 and R_4. Thus, the minimum load current on the output is about 7mA.

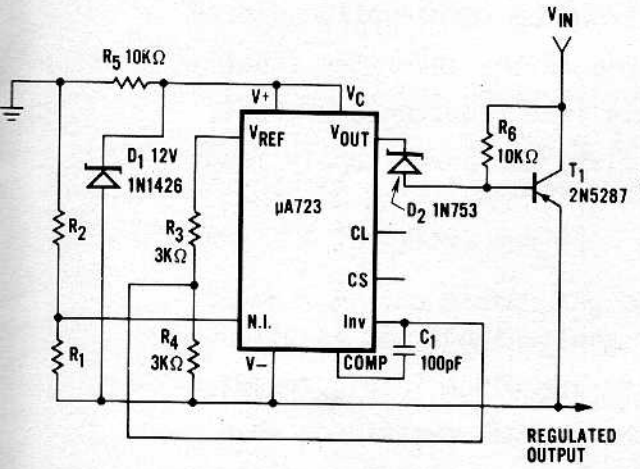
Another application of "floating" operation is a negative voltage regulator (Figure 22). This capability is somewhat unique to the µA723 in that most monolithic voltage regulators will not operate from unisolated negative D.C. supplies. The resistors shown provide outputs of -15 volts. If R_1 is a fixed 3.5KΩ, then R_2 for various negative outputs can be calculated from:

$$R_2 = (Vo - 3.5)\ 10^3 \qquad (5)$$

This circuit has good line rejection because changes in the unregulated output do not change the V^+ to V^- voltage of the µA723. Better line rejection can be obtained by replacing R_5 by an FET current source. The current through R_5 must be greater than the maximum base current of Q_1.

FIGURE 22

NEGATIVE FLOATING REGULATOR

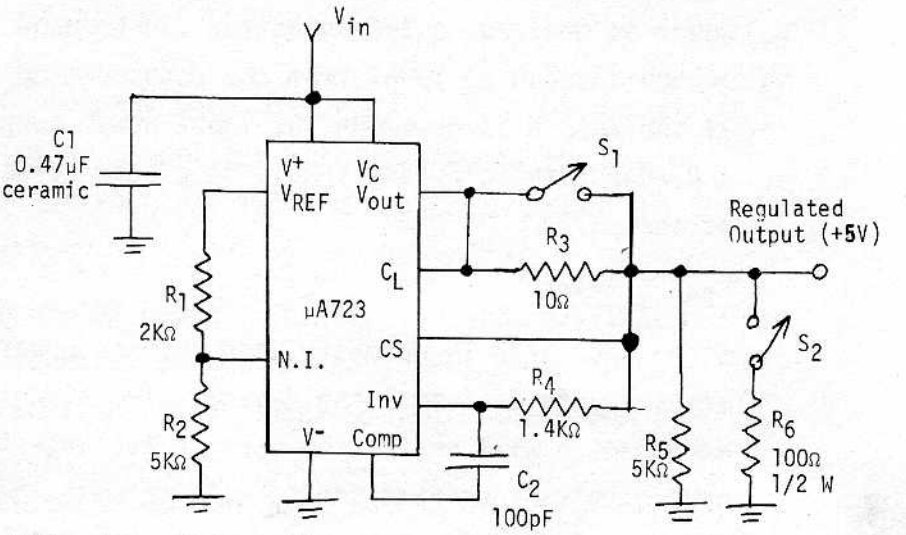


TYPICAL PERFORMANCE

Regulated Output Voltage	−100 V
Line Regulation ($\Delta V_{IN} = 20$ V)	30 mV
Load Regulation (ΔI_L=100 mA)	20 mV

FIGURE 23

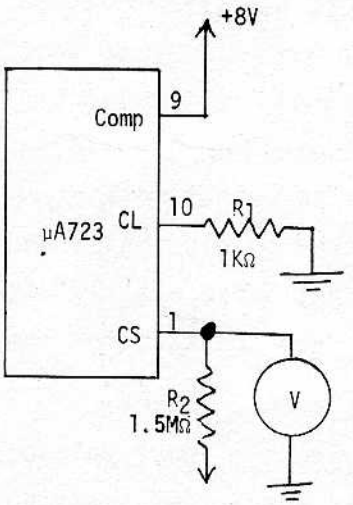
Simplified Tester Schematic



NOTE: All resistors ±1%

FIGURE 24

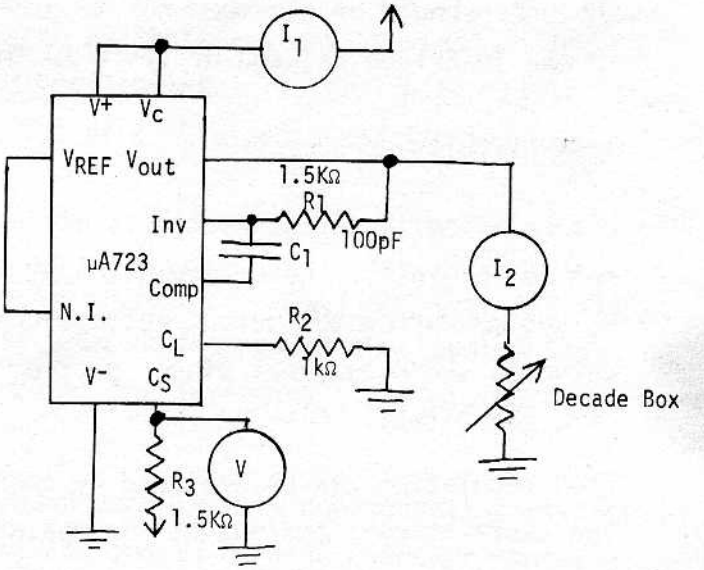
Calibration Circuit



NOTE: All other pins are not connected.

FIGURE 25

Thermal Resistance Measurement Circuit



Frequency Compensation

When used without external pass transistors, C_1 = 100pF is more than adequate to assure frequency stability of the μA723. With external pass transistors it is usually necessary to increase C_1 to about 500pF. If minimum component count is desired, a 1nF capacitor can be used from the compensation pin to ground instead of 100pf from the compensation pin to the inverting input. If there is a large amount of input power supply lead inductance present, a 0.46μF ceramic bypass should be placed across the two power supply leads of the μA723.

Heat Sinking

Since the μA723 is normally used in high power applications, it is often necessary to heat sink the device. Two circuits are given in Figures 24 and 25 which will enable the user to evaluate the thermal resistance when used with various heat sinks. The circuit in Figure 24 is used to calibrate the V_{BE} of Q_{16} with temperature. V_{BE} is measured in an oven at the current-sense pin as the ambient temperature is varied. After calibrating V_{BE}, the circuit in Figure 25 is used to vary this power dissipation while the ambient temperature remains fixed. The thermal resistance is calculated from the following.

$$\text{Thermal Resistance} = \frac{\Delta T}{\Delta P} \text{ °C/W} \quad (TC1)$$

The power dissipation can be calculated from the formula:

$$\Delta P = 7I_2 + 30\ (I_1 - I_2) \qquad (TC2)$$

The user should be cautious not to exceed a junction temperature of 150°C in the TO-5 type package or 125°C in the DIP.

Test Circuits

A simplified tester schematic is given in Figure 23. The output voltage is set for +5 volts. Load regulation at 50mA can be checked by closing S_1 and S_2 and measuring the output voltage change. This may not agree exactly with value on the data sheet since junction temperature is held constant for the data sheet test.

Line regulation can be measured by opening S_2 and varying the input voltage. The short circuit current can be measured by opening S_1 and S_2 and shorting the output to ground through an ammeter. Other tests such as ripple rejection, noise, temperature coefficient, etc. can be easily performed.

LINEAR VOLTAGE REGULATORS USING A NEW MONOLITHIC CIRCUIT

by Robert D. Ricks

Introduction

A new monolithic voltage regulator has been developed by Fairchild Semiconductor. Through the wide range of options incorporated in the design, the device will function over the complete range of voltages normally required in system applications.

Figure 1 is the block diagram of the device. Unlike circuits available up to this time, several interconnection options have been provided to extend capability in various applications. These options include:

1. The internally generated reference voltage is buffered and brought out for use in a variety of connections.
2. Both sides of the error amplifier are addressable to allow an additional flexibility for use with negative supplies or high voltages.
3. The collector of the internal power transistor is separated from the internal circuitry and available externally.
4. An offsetting zener diode is provided for minimum external parts count in the floating configurations when using the DIP package versions.

Regulator Configurations

To illustrate the advantages represented by those options, several different configurations have been designed and constructed. The following illustrations and discussion gives a brief description of each circuit and its measured regulation performance.

CIRCUIT #1 (2 to 8 volt, medium current)

This is the standard low voltage self-contained regulator configuration. The resistor divider from V_{Ref} is used so that no attenuation of the output voltage charges is required at the inverting input of the comparison amplifier.

The frequency compensation to ground used in this configuration assures stability with minimum part count and should be used whenever impedance

FIGURE 1

EQUIVALENT CIRCUIT

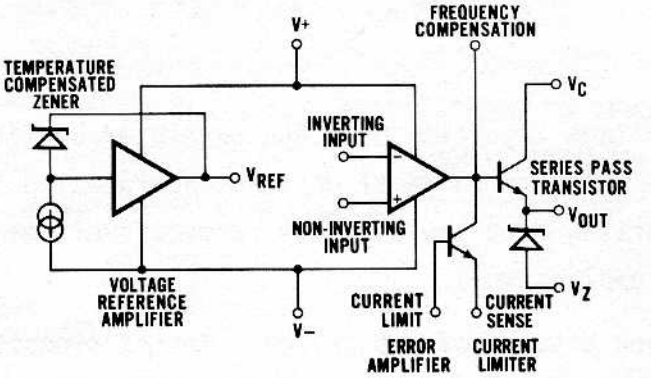


FIGURE 2

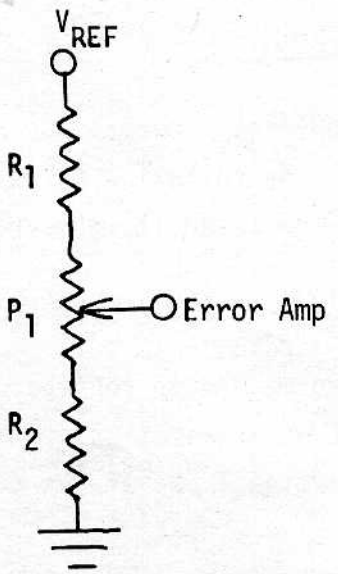
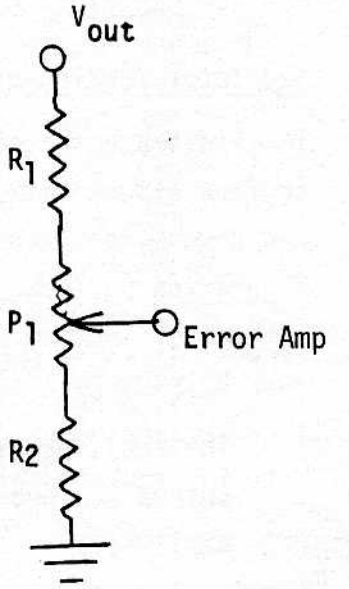
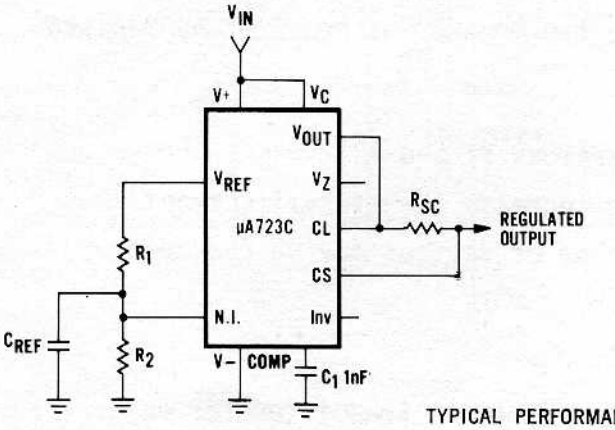


FIGURE 3



Circuit #1

BASIC LOW VOLTAGE REGULATOR
(V_{out} = 2 to 7 Volts)



TYPICAL PERFORMANCE

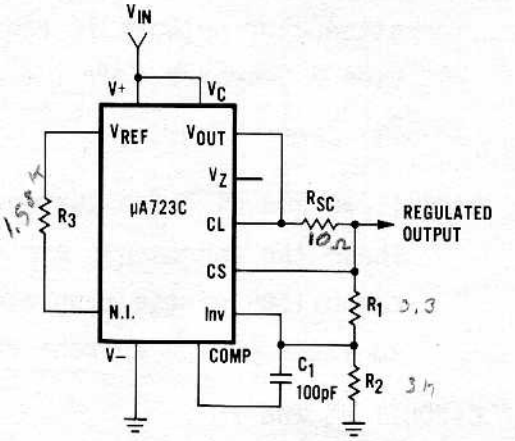
Regulated Output Voltage	5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Note: $R_3 = \frac{R_1 R_2}{R_1+R_2}$ for minimum temperature drift.

R_3 may be eliminated for minimum component count.

Circuit #2

BASIC HIGH VOLTAGE REGULATOR
(V_{out} = 7 to 37 Volts)



TYPICAL PERFORMANCE

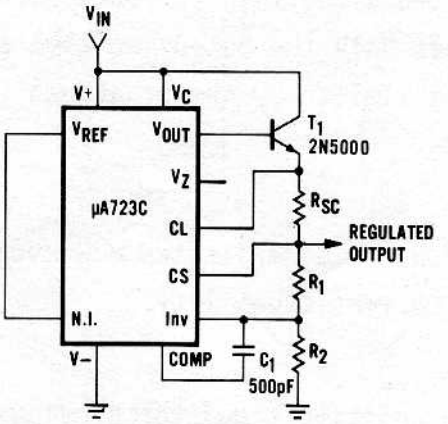
Regulated Output Voltage	15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5 mV
Load Regulation (ΔI_L=50 mA)	4.5 mV

Note: $R_3 = \frac{R_1 R_2}{R_1+R_2}$ for minimum temperature drift.

R_3 may be eliminated for minimum component count.

Circuit #3

POSITIVE VOLTAGE REGULATOR
(External NPN Pass Transistor)

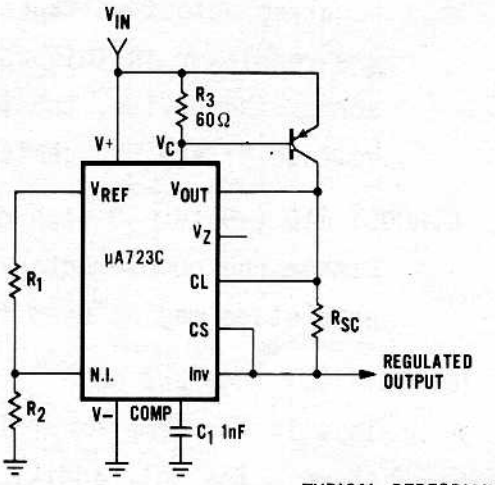


TYPICAL PERFORMANCE

Regulated Output Voltage	+15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5 mV
Load Regulation (ΔI_L = 1 A)	15 mV

Circuit #4

POSITIVE VOLTAGE REGULATOR
(External PNP Pass Transistor)



TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L = 1 A)	5 mV

is not required between the output and the inverting input.

CIRCUIT #2 (7 to 37 volt, medium current)

To regulate any voltage above the internal reference voltage, a resistor attenuator network is required as shown. The frequency compensation uses a feedback from the output using the breakpoint provided by resistor R_1.

CIRCUIT #3 and #4 (high current circuit versions #1 and #2)

These two approaches are available to increase the overall current capability of the regulator. Any number of devices may be cascaded to satisfy high current requirements.

CIRCUIT #5 and #6

These configurations trade off the current limit transistor for an increase in power supply rejection. Using the connection shown, line rejections of 100 db may be obtained. When used as a zener, the current limit transistor's base-emitter current should be limited to 5mA.

CIRCUIT #7 and #8 (+40 V and up)

The μA723 may be used to directly regulate hundreds of volts using the configuration shown. When using this floating mode of operation the current drawn from the V_{REF} pin should be limited to 5mA. This will allow voltage programming resistors of 200 ohms per volt.

CIRCUIT #9 (-9 to -40V)

Negative output voltages may be regulated using this approach. Since the regulator in this configuration sees only the output voltage applied across the device, the input voltage is limited by the breakdown voltage of the PNP series pass elements.

CIRCUIT #10 (-9 to -40 high current)

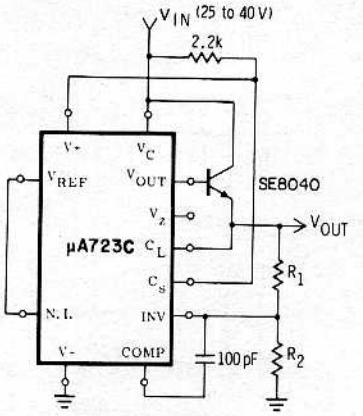
Either the complementary connection shown or a darlington PNP current gain stage may be used for additional current capability.

CIRCUIT #11 (-40 and up)

This is the complement to the floating positive regulator previously shown. The only additional component necessary is the zener diode which is required to limit the voltage seen by the device to less than 40 volts.

Circuit #5

HIGH LINE REJECTION POSITIVE REGULATOR

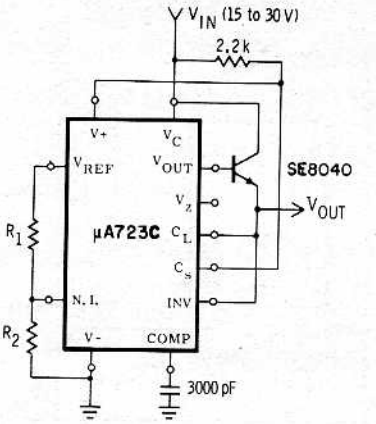


Typical Regulation Data

Parameter	Δ Change	Output Change
1) V_{OUT}	----	+15 V
2) Line Reg.	15 V	< 1 mV
3) Load Reg.	50 mA	1 mV

Circuit #6

HIGH LINE REJECTION POSITIVE REGULATOR

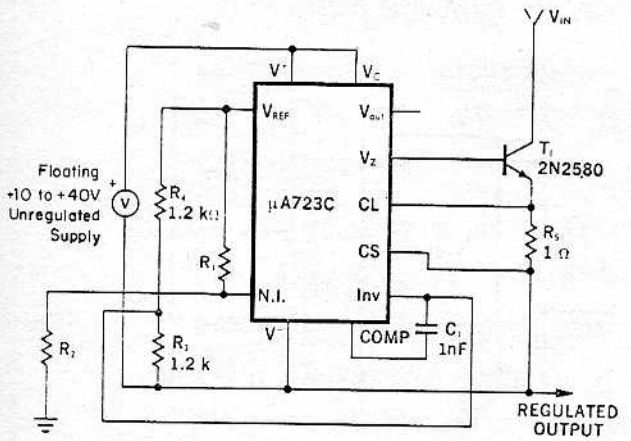


Typical Regulation Data

Parameter	Δ Change	Output Change
1) V_{OUT}	----	+ 5 V
2) Line Reg.	15 V	< 1 mV
3) Load Reg.	50 mA	10 mV

Circuit #7

POSITIVE FLOATING REGULATOR

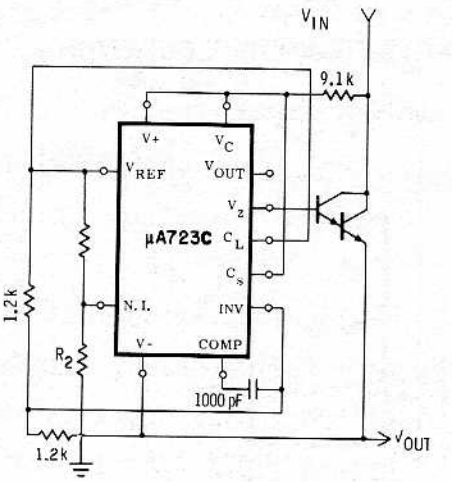


TYPICAL PERFORMANCE

Regulated Output Voltage	+100 V
Line Regulation (ΔV_{IN} = 20 V)	15 mV
Load Regulation (ΔI_L = 50 mA)	20 mV

Circuit #8

POSITIVE FLOATING REGULATOR

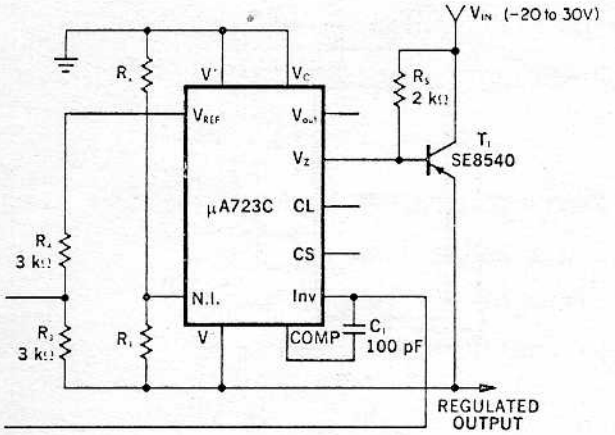


Typical Regulation Data

Parameter	Δ Change	Output Change
1) V_{OUT}	----	+100 V
2) Line Reg.	20 V	15 mV
3) Load Reg	100 mA	20 mV

Circuit #9

NEGATIVE VOLTAGE REGULATOR

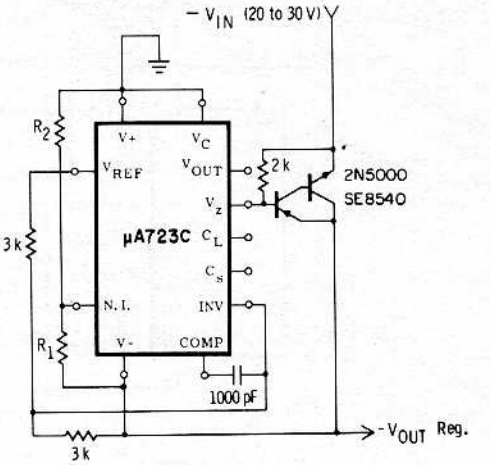


TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1 mV
Load Regulation ($\Delta I_L = 100$ mA)	2 mV

Circuit #10

NEGATIVE HIGH CURRENT VOLTAGE REGULATOR

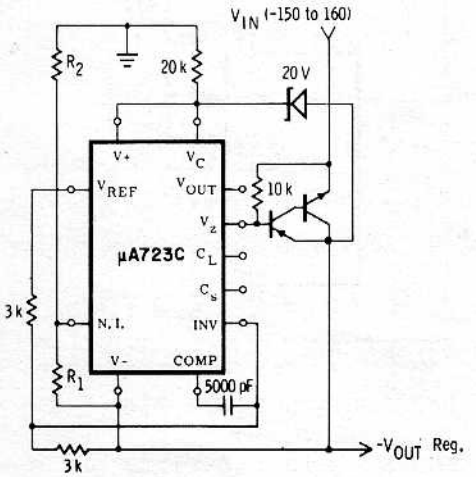


Typical Regulation Data

Parameter	Δ Change	Output Change
1) V_{OUT}	----	-15 V
2) Line Reg.	10 V	4 mV
3) Load Reg.	Lamp	2 mV

Circuit #11

NEGATIVE FLOATING REGULATOR

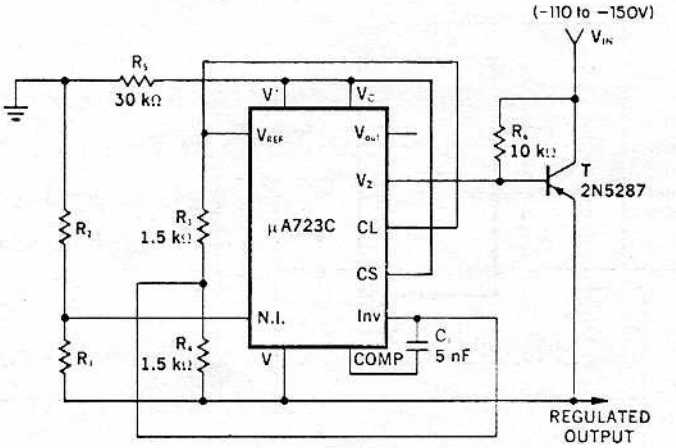


Typical Regulation Data

Parameter	Δ Change	Output Change
1) V_{OUT}	----	-100 V
2) Line Reg.	20 V	30 mV
3) Load Reg.	100 mA	20 mV

Circuit #12

NEGATIVE FLOATING REGULATOR

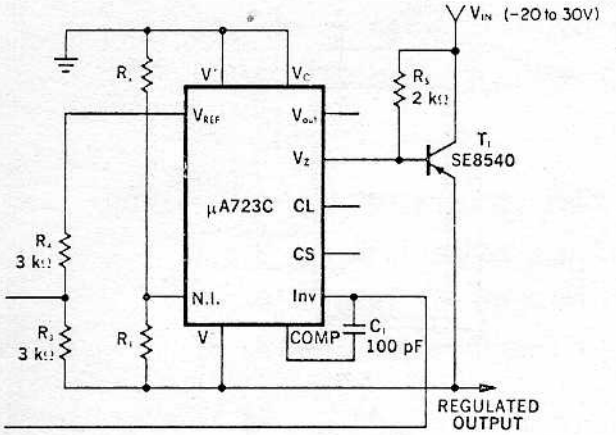


TYPICAL PERFORMANCE

Regulated Output Voltage	−100 V
Line Regulation ($\Delta V_{IN} = 20$ V)	30 mV
Load Regulation (ΔI_L=100 mA)	20 mV

Circuit #9

NEGATIVE VOLTAGE REGULATOR

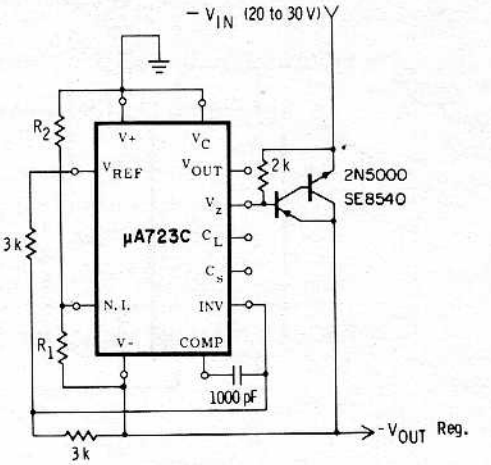


TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1 mV
Load Regulation ($\Delta I_L = 100$ mA)	2 mV

Circuit #10

NEGATIVE HIGH CURRENT VOLTAGE REGULATOR

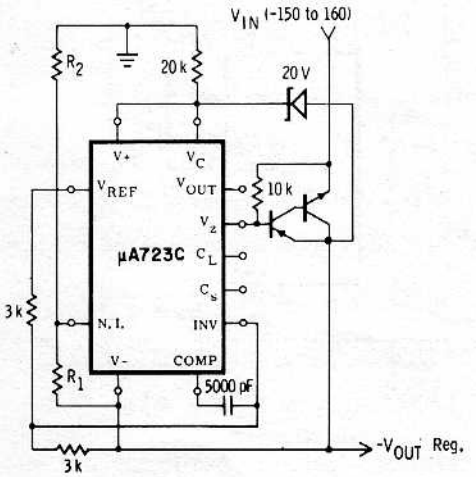


Typical Regulation Data

Parameter	ΔChange	Output Change
1) V_{OUT}	----	-15 V
2) Line Reg.	10 V	4 mV
3) Load Reg.	Lamp	2 mV

Circuit #11

NEGATIVE FLOATING REGULATOR

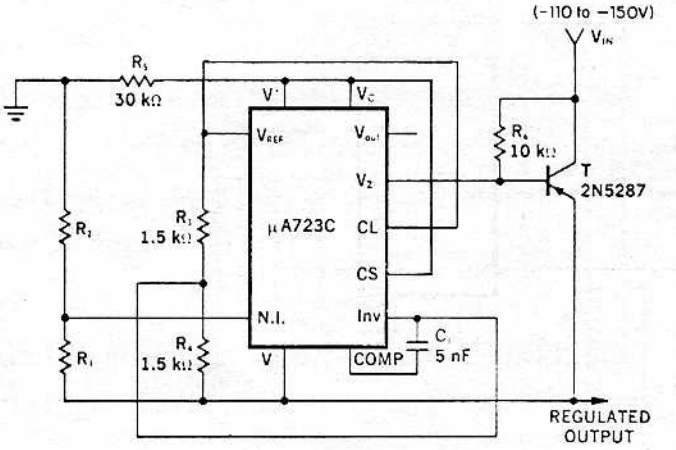


Typical Regulation Data

Parameter	ΔChange	Output Change
1) V_{OUT}	----	-100 V
2) Line Reg.	20 V	30 mV
3) Load Reg.	100 mA	20 mV

Circuit #12

NEGATIVE FLOATING REGULATOR



TYPICAL PERFORMANCE

Regulated Output Voltage	−100 V
Line Regulation ($\Delta V_{IN} = 20$ V)	30 mV
Load Regulation (ΔI_L=100 mA)	20 mV

CIRCUIT #12 (-40 and up)

Another negative regulator in which the base-emitter junction of the internal current limit transistor is used as a zener diode and added to the V_{REF} output to achieve a 14 volt stabilized voltage source for the control portion of the regulator.

CIRCUIT #13 (-15V High Line Rejection)

In those cases in which the normal 65 to 70 db line rejection is not sufficient, the addition of the FET constant current source results in the complement to the positive voltage 100 db line rejection regulator (circuit #5).

CIRCUIT #14 (Remote Shutdown)

Where remote shutoff capability is required, the compensation pin may be pulled down as shown by an external transistor. Where current limiting is not required, the internal transistor may be used by grounding the C_L pin and driving the C_S pin with approximately 1 mA base current.

CIRCUIT #15 (Fold-Back Current Limiter)

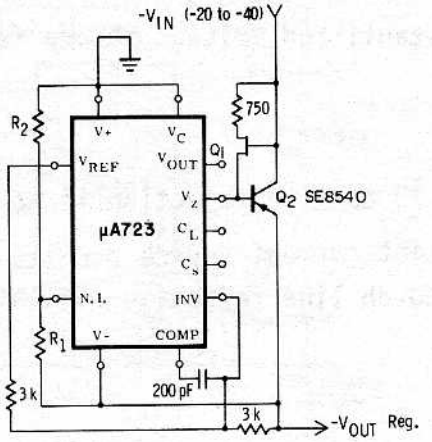
In many cases the dissipation which occurs under current limited short circuit conditions is excessive and, if accounted for, results in excessive heat sink area. The enclusion of positive feedback as shown in the current limit circuitry produces short circuit currents which approach zero. Table II provides the formula for calculation of the short circuit current knee.

CIRCUIT #16 (Low Voltage Negative Regulator)

The μA723 requires a minimum voltage across the device for satisfactory operation. Therefore, when regulating negative voltages less than nine volts it is necessary to connect the device as shown to any available positive source such that the voltage across the unit is always in excess of the required nine volts.

Circuit #13

HIGH LINE REJECTION NEGATIVE REGULATOR



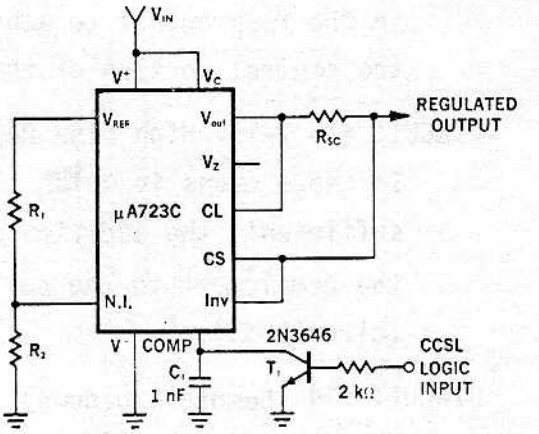
NOTE: Q_1 is FE0654A or FE0654B

Typical Regulation Data

Parameter	ΔChange	Output Change
1) V_{OUT}	----	-15 V
2) Line Reg.	20 V	< 1 mV
3) Load Reg.	100 mA	2 mV

Circuit #14

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING



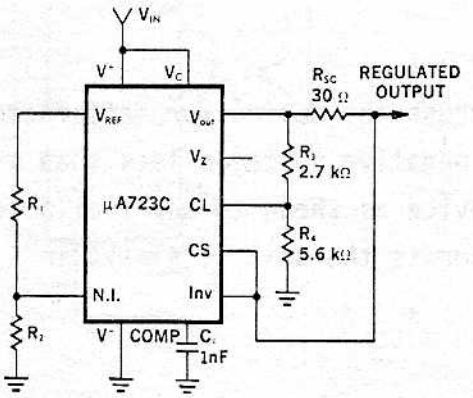
Note: Current limit transistor may be used for shutdown if current limiting is not required.

TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Circuit #15

FOLDBACK CURRENT LIMITING

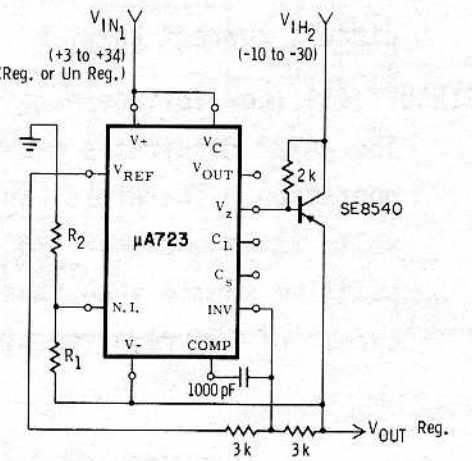


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L = 10 mA)	1 mV
Current Limit Knee	20 mA

Circuit #16

LOW VOLTAGE NEGATIVE REGULATOR

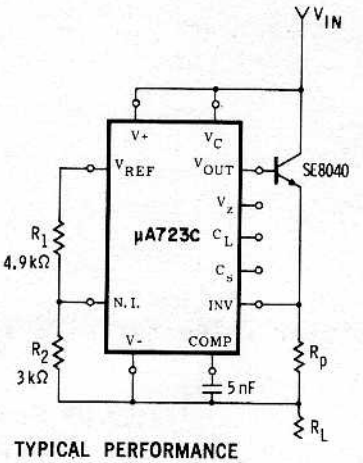


Typical Regulation Data

Parameter	Change	Output Change
1) V_{OUT}	----	-6 V
2) Line Reg.	10 V	4 mV
3) Load Reg.	100 mA	2 mV

Circuit #17

CONSTANT CURRENT SOURCE

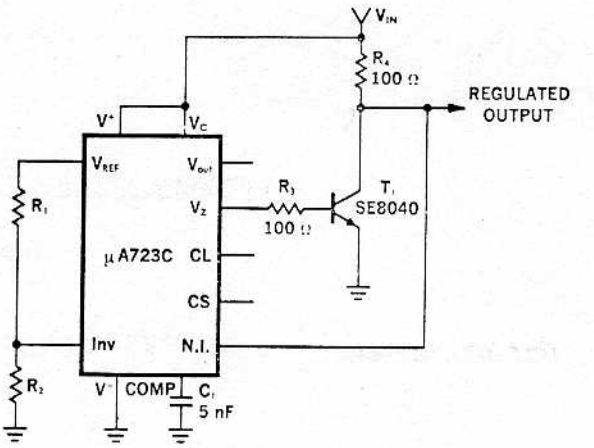


TYPICAL PERFORMANCE

		mA
Output Current		
Line Regulation (ΔV_{IN} =	5V)	0.3 mV
Load Regulation (ΔI_L =	200Ω)	0.2mV

Circuit #18

SHUNT REGULATOR



TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation (ΔV_{IN} = 10 V)	2 mV
Load Regulation (ΔI_L = 100 mA)	5 mV

CIRCUIT #17 (Current Regulator)

Current regulator may be constructed as shown. Line regulation deteriorates with programmed currents under 10mA as both the programmed current and the quiescent device current flow through the load. See Table II for the necessary formulas.

CIRCUIT #18 (Shunt Regulator)

Shunt regulation is accomplished as shown. Care should be executed in the power dissipation calculation of the current limiting resistor as this is the only circuit presented in which a passive element outside the load resistor dissipates high power.

Output Voltage Levels

Table I and II have been provided to assist the user in his applications. Table I lists the most commonly used system supply voltages and the appropriate divider values. In case a voltage level outside of those listed in Table I is required, then the formulas given in Table II may be used to generate the proper divider values.

Conclusion

A new monolithic voltage regulator has been presented with sufficient circuit configurations to demonstrate the flexibility of the device.

Using the information presented in this paper, power supplies of any voltage and/or current level may be quickly and conveniently constructed.

RECOMMENDED RESISTOR DIVIDER VALUES

Table 1

Output Voltage	Fig. #	Circuit Numbers	Resistor Value for ±10% V_{OUT}		
			R_1	P_1	R_2
+3.0	2	1,6	1.8K	500	1.2K
+3.6	2	1,6	1.5K	500	1.5K
+5.0	2	1,6	750	500	2.2K
+6.0	2	1,6	500	500	2.7K
+9.0	3	2,3,4,5	750	1K	2.7K
+12.0	3	2,3,4,5	2K	1K	3K
+15.0	3	2,3,4,5	3.3K	1K	3K
+28.0	3	2,3,4,5	5.6K	1K	2K
+48.0	3	7,8	0	10K	39K
+75	3	7,8	0	10K	68K
+100	3	7,8	0	10K	91K
+250	3	7,8	0	10K	240K
-6	3	16	1.2K	500	750
-9	3	9,10,13	1.2K	500	2.0K
-12	3	9,10,13	1.2K	500	3.3K
-15	3	9,10,13	1.2K	500	4.3K
-28	3	9,10,13	1.2K	500	10K
-45	3	11,12	0	10K	33K
-100	3	11,12	0	10K	91K
-250	3	11,12	0	10K	240K

TABLE II

Parameter	Circuits	Formula
Short Circuit current		$I_{Lim} = \frac{0.7}{R_{sc}}$ (in ohms)
Fold back current limit	#15	I_{Lim} = (Knee) $= \frac{1.0}{R_{sc}}$
Current regulator	#17	$I_{out} = \frac{3}{R_p}$ (in ohms)
		V_{in} (min.) = 9V + R_L I_{out}
V_{out}	1,6	$V_{out} = \frac{R_1}{R_1+R_2}$ X 7V (Where $R_1 + R_2 > 1.5K$)
V_{out}	2,3,4,5	$V_{out} = \frac{R_1 + R_2}{R_2}$ X 7V
V_{out}	7,8	$V_{out} = \frac{3.5\ (R_2 + R_1)}{R_1}$
V_{out}	16	$V_{out} = \frac{3.5\ (R_2 + R_1)}{R_1}$
V_{out}	9,10,13	$V_{out} = \frac{3.5\ (R_2 + R_1)}{R_1}$
V_{out}	11,12	$V_{out} = \frac{3.5\ (R_2 + R_1)}{R_1}$

SWITCHING REGULATOR DESIGN USING THE μA723 MONOLITHIC INTEGRATED VOLTAGE REGULATOR

by Michael J. English

The switching mode voltage regulator offers the advantage of high efficiency over the more common series or shunt regulation schemes. This is particularly apparent when there is a large difference between the input voltage and the regulated output voltage. Consider, for example, a voltage regulator with 28 volts input and an output of 5 volts at one ampere. A conventional series regulator would require a drop of 23 volts across the pass transistor. Thus, 23 watts would be wasted, and the efficiency would be only 18%. Switching regulators, however, can be simply designed to give efficiencies greater than 75% under the same input and output restrictions. As with series regulators, greater efficiencies can be realized when there is less of a difference between input and output voltages.

Switching regulators may also be useful in applications where cost, rather than efficiency, is the prime design criteria. The designer may trade the cost of a high power series pass transistor for a slight increase in circuit complexity that will allow the use of lower power switching transistors.

Operation of Switching Regulators

The operation of the switching regulator may be explained by referring to Figure 1. The switch transistor, Q_1, is operated only in saturation or in cut-off so that power dissipation is kept to a minimum. Diode D_1 conducts during the time that Q_1 is cut-off, thus maintaining current flow in inductor L_1.

When Q_1 is turned on, D_1 is reverse biased, and does not conduct. The current in L_1 will increase linearly according to the relation:

$$E_{in} - E_{out} = L_1 \frac{\Delta i_L}{t_{on}}$$

This current flows in the load, and charges capicitor C_1. The voltage at the non-inverting input to the error amplifier is given approximately by:

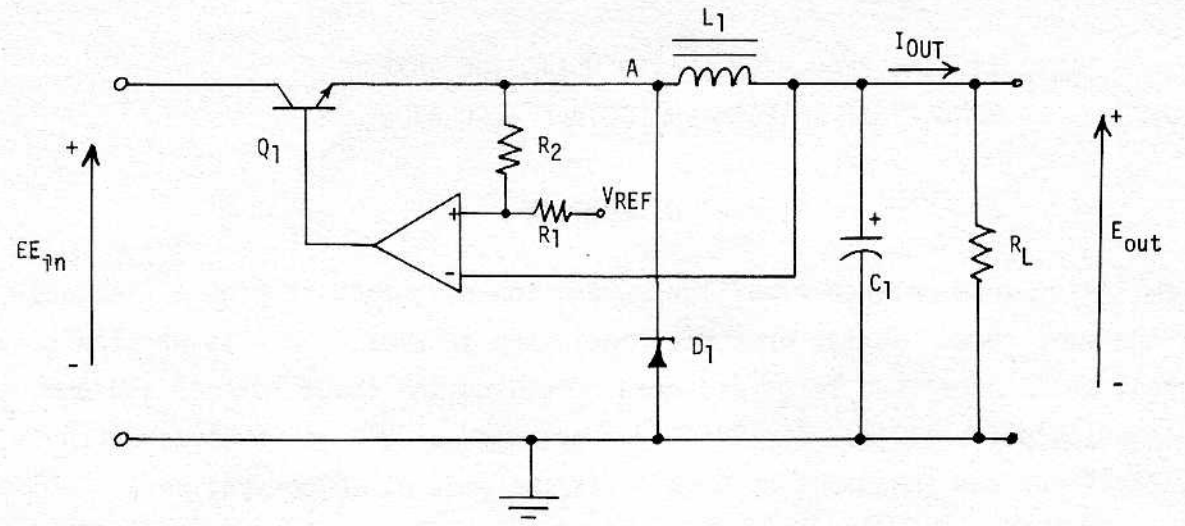


FIGURE 1: Basic Switching Regulator Circuit

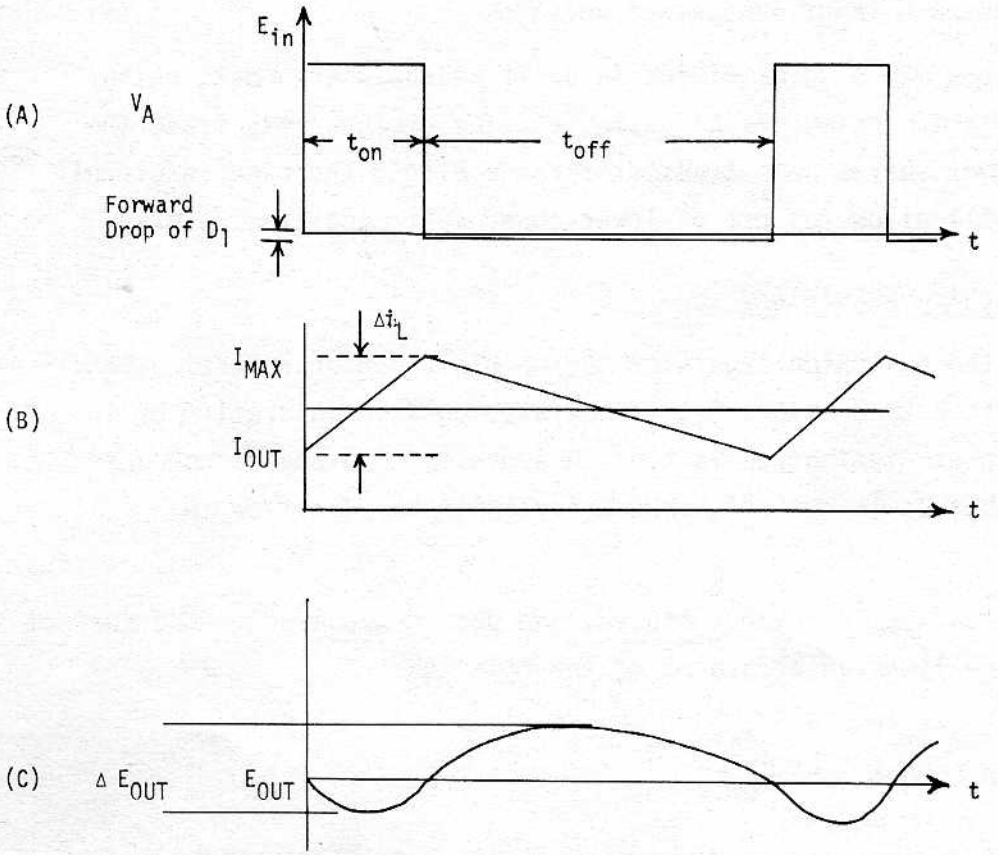


FIGURE 2: A. Voltage at Point A, Figure 1
B. Inductor Current
C. Output Voltage

FIGURE 3

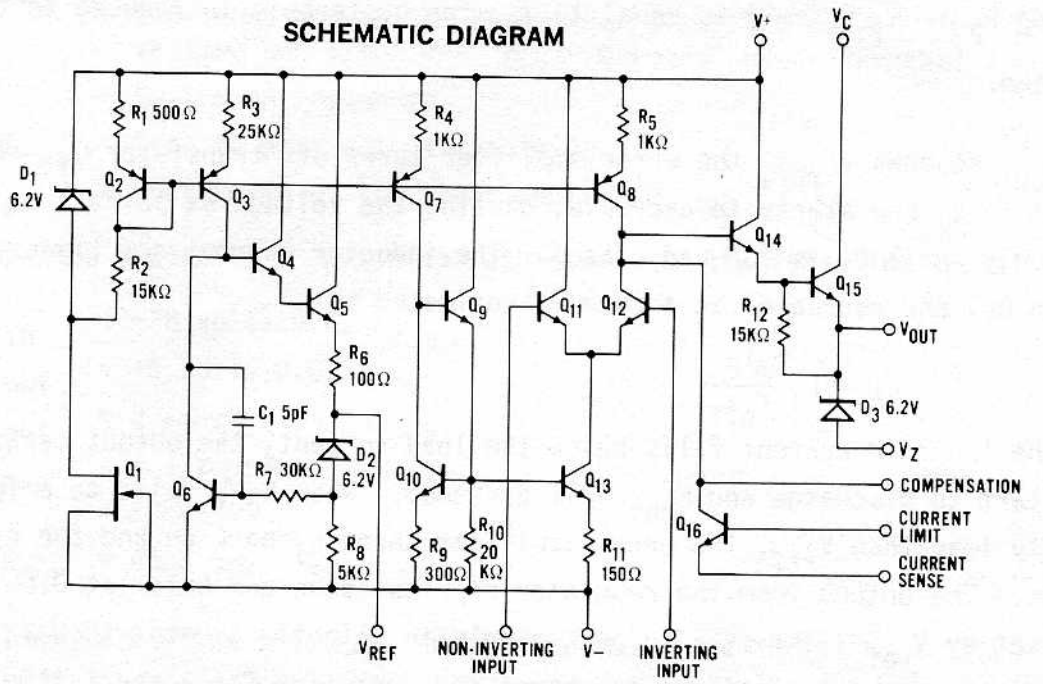
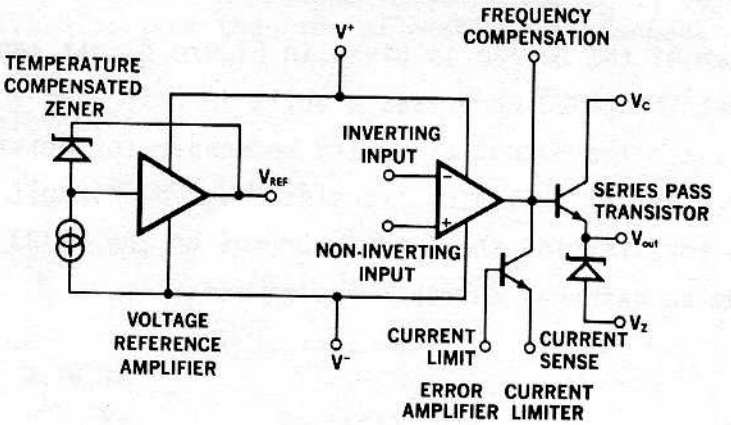


FIGURE 4



$$V'_{ref} = V_{ref} + E_{in} \left(\frac{R_1}{R_2}\right)$$

assuming $R_2 >> R_1$ $E_{in} \left(\frac{R_1}{R_2}\right)$ is equal to V_H, the hysteresis introduced to the error amp.

When E_{out} reaches V'_{ref}, the error amplifier turns off transistor Q_1. The current in L_1 now starts to decrease, causing the voltage at point A to swing negatively until D_1 is forward biased. The inductor current now flows through D_1, and decreases at a rate approximated by:

$$E_\phi = L_1 \frac{\Delta i_L}{t_{off}}$$

When the inductor current falls below the load current, the output capacitor will start to discharge and E_{out} will decrease. When E_{out} falls to a level slightly less than V_{ref}, the error amplifier turns Q_1 back on and the cycle repeats. The output from the regulator ripples above and below at D.C. level set by V_{ref}. The peak to peak ripple is slightly greater than V_H, as the inductor current continues to charge the capacitor for a short time after A is switched off. The significant voltage and current wave forms are given in Figure 2.

Using the μA723 in Switching Regulators

The μA723 is a monolithic integrated circuit designed for use as a voltage regulator. Although the circuit is intended primarily for use as a series type linear regulator, it contains all the elements needed to control the operation of a switching regulator. A schematic of the μA723 is shown in Figure 3.

A simplified diagram of the device is given in Figure 4. It can be seen from the figure that the μA723 comprises a built in reference voltage source, an error amplifier, and the output circuitry necessary for driving various configurations for external switching transistors. The circuit also includes provision for limiting the output current of the μA723 by driving the base of Q_2 from an external current sensing resistor.

Design Example

Definition of Terms:

E_{in} = Unregulated D.C. input voltage
E_{out} = Regulated output voltage

I_{out} = D.C. output current of the regulator

I_{max} = Maximum inductor current (hence also the maximum non-transient switch transistor current and the maximum non-transient "free-wheeling" diode current)

f = Switching frequency

ΔE_{out} = Peak to peak output ripple

V_H = Hysteresis of the error amplifier

Consider the design of a switching regulator with the following specifications:

E_{in} = +28 volts D.C.

E_{out} = +5 volts D.C.

I_{out} = 2 amperes

I_{max} = 2.1 amperes

f = 20KHz

ΔE_{out} = 40mV p-p

a) Calculate the required inductance, L_1, using relation

$$L_1 = \frac{(E_{in} - E_{out})\ t_{on}}{2\ (I_{max} - I_{out})} \quad \text{henries}$$

where

$$t_{on} = \frac{E_{out}}{E_{in}}\ \frac{1}{f}$$

thus

$$L_1 = \frac{(28 - 5)}{+\ (2.1 - 2)}\ \left(\frac{5}{28}\right)\ \left(\frac{1}{2 \times 10^4}\right) = 1.25\text{mH}$$

b) Choose a value for V_H. (Controlling the hysterisis provides a convenient means for trimming the operating frequency as well as supplying positive feedback to enhance switching action. A reasonable value for V_H is 10 to 20 millivolts less than the allowable peak to peak output ripple.)

For example, take

$$V_H = 30 \text{ millivolts}$$

also

$$V_H \cong E_{in}\ \frac{R_1}{R_2} \quad (R_2 >> R_1)$$

so if

$$R_1 = 1\text{K}$$

$$R_2 = \frac{V_{in}}{V_H} \quad R_1 = \frac{28\ (10^3)}{30 \times 10^{-3}}$$

$$R_2 \cong 1 \text{ Meg}$$

Dan 1147-122et

c) Calculate the value of capacitor C_1 from

$$C_1 = \frac{(E_{in} - E_{out})\, E_{out}}{8L\, f^2\, E_{in}\, (\Delta V_{out} - V_H)}$$

$$C_1 = \frac{(28 - 5)\,(5)}{8\,(1.25 \times 10^{-3})\,(2 \times 10^4)^2\, 28\,(40 - 30)\,(10^{-3})}$$

$$C_1 = 102.5\ \mu fd$$

The actual component values used were

$L_1 = 1.2mH$

$C_1 = 100\mu fd$

The final form of the circuit is shown in Figure 5. The 51 ohm resistor, R_5, limits the base drive of Q_2 to about 15mA by using the internal current limiting of the μA723. Since E_{out} is less than the 7.1 volt reference voltage supplied by the μA723, the internal reference is divided down to 5 volts by R_3 and R_4.

If the required output were greater than V_{ref}, the divider would be attached to the output voltage, the division ratio calculated to divide the desired output down to the reference level, and the reference applied directly to the error amplifier.

C_2 maintains a constant voltage across R_4. V_H is provided by the resistive divider composed of R_1 and R_2.

The efficiency of this circuit 73% at I_{out} = 2 amperes. When I_{out} is 1 ampere, the efficiency is 78%.

Figure 6 shows a circuit for a switching regulator with negative output voltage. Operation is similar to the positive regulator circuit, except the drive signal to the switching transistors is supplied from the V_{zener} output of the μA723. The zener provides the necessary level shifting required to maintain biasing of the regulator. (μA723's in the metal can package do not have a V_{zener} output. When using these devices, it would be necessary to add an external 6.2 volt zener between V_{out} and the switch transistors).

This circuit configuration is useful for output voltages more negative than -9 volts. This is because the μA723 is operated from the output of the regulator and requires at least 9 volts across its' power terminals for

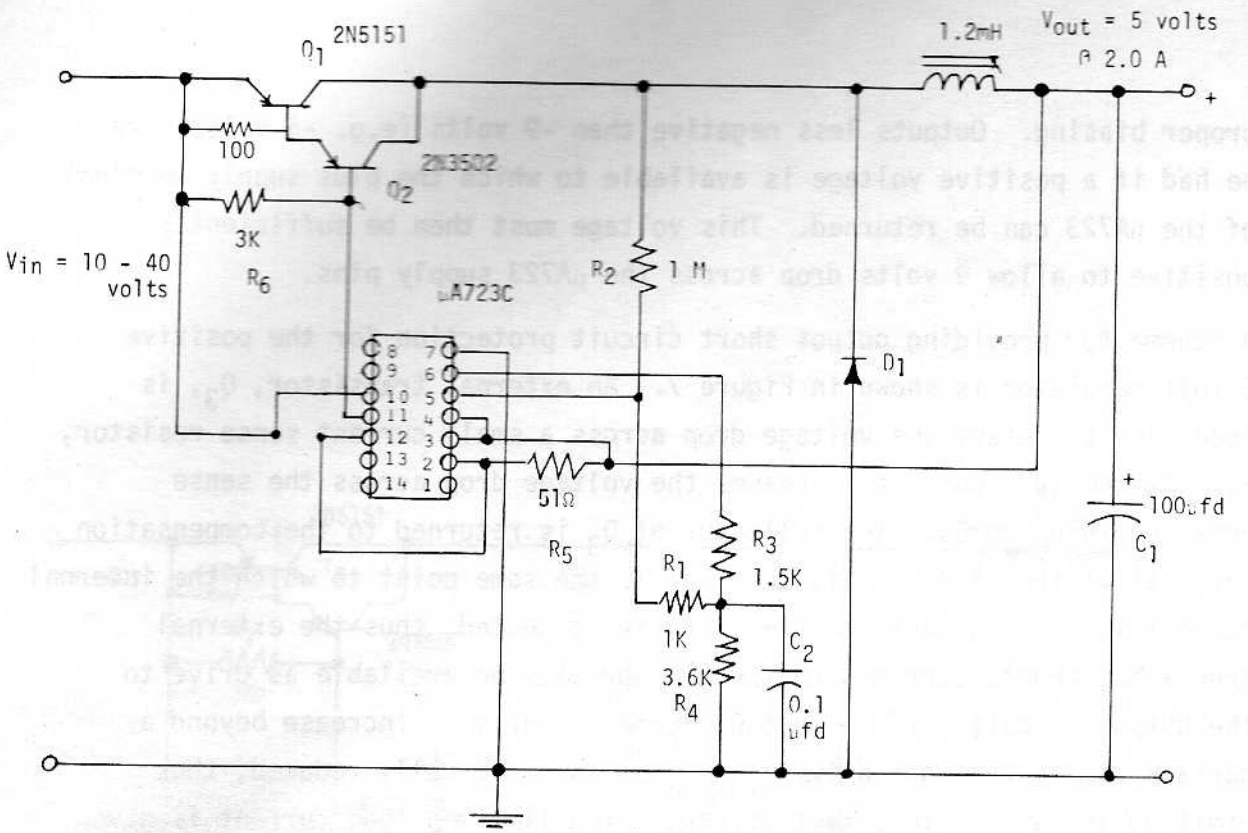


FIGURE 5: Positive Switching Regulator

NOTE: L_1 is 40 turns #20 enameled copper wire wound on a Ferrox cube P36/22-3B7 pot core with 0.009" air gap or equivalent

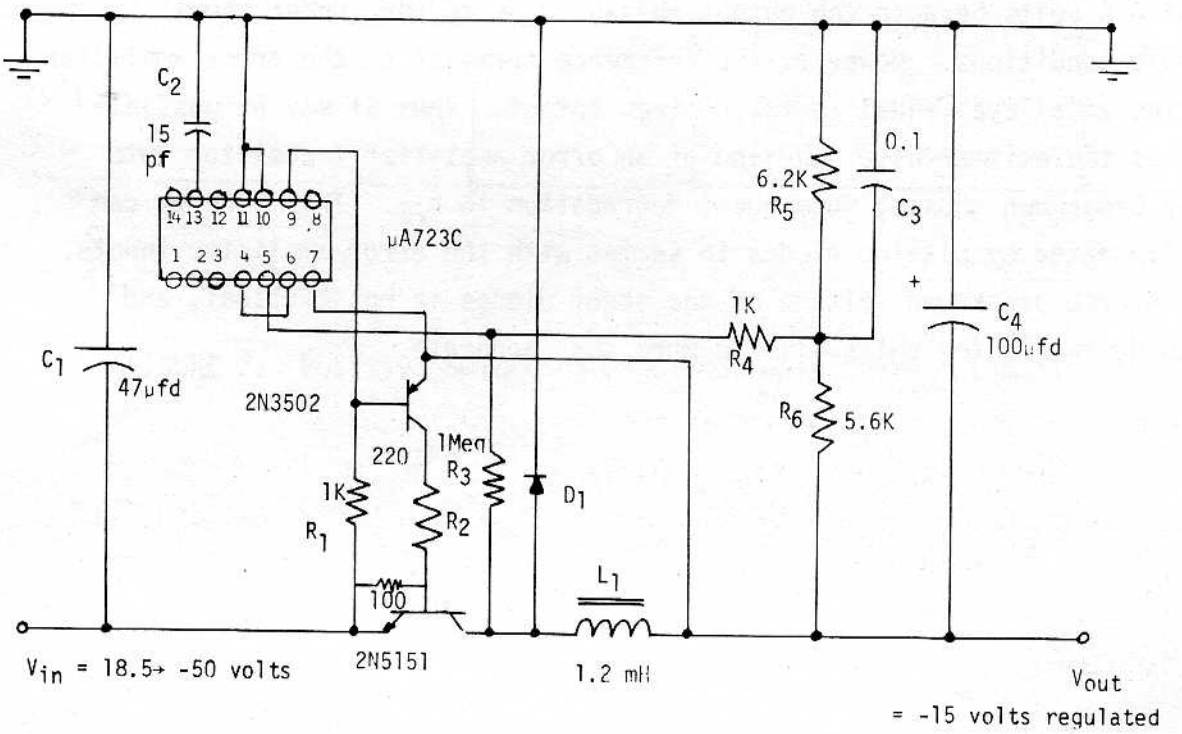


FIGURE 6: Negative Switching Regulator

proper biasing. Outputs less negative than -9 volts (e.g. -5 volts) can be had if a positive voltage is available to which the plus supply terminal of the μA723 can be returned. This voltage must then be sufficiently positive to allow 9 volts drop across the μA723 supply pins.

A scheme for providing output short circuit protection for the positive 5 volt regulator is shown in Figure 7. An external transistor, Q_3, is connected to detect the voltage drop across a small current sense resistor, R_7. As the load current increases the voltage drop across the sense resistor turns on Q_3. The collector of Q_3 is returned to the compensation terminal of the μA723. This terminal is the same point to which the internal current limiting circuit of the μA723 is connected, thus the external transistor shunts current that would normally be available as drive to the output circuit. If the output current starts to increase beyond a curtain limit, the base drive to Q_1 - Q_2 is drastically reduced, thus limiting the available output current. The limiting load current is given approximately by:

$$I_{LIM} = \frac{V_{be}}{R_7} \cong \frac{0.7}{R_7} \qquad \text{for silicon transistors}$$

This current limiting scheme is only useful for output voltages less than about 6.5 volts because the output voltage goes to zero under short circuit conditions. However, the reference terminal of the error amplifier remains at a level equal to the desired output. Thus it may be possible to bias the emitter-base junction of an error amplifier transistor into zener breakdown causing subsequent degradation in h_{FE}. This problem can be eliminated by placing diodes in series with the error amplifier inputs. The reverse breakdown voltage of the added diodes is not critical, and anything over a few volts will be more than adequate.

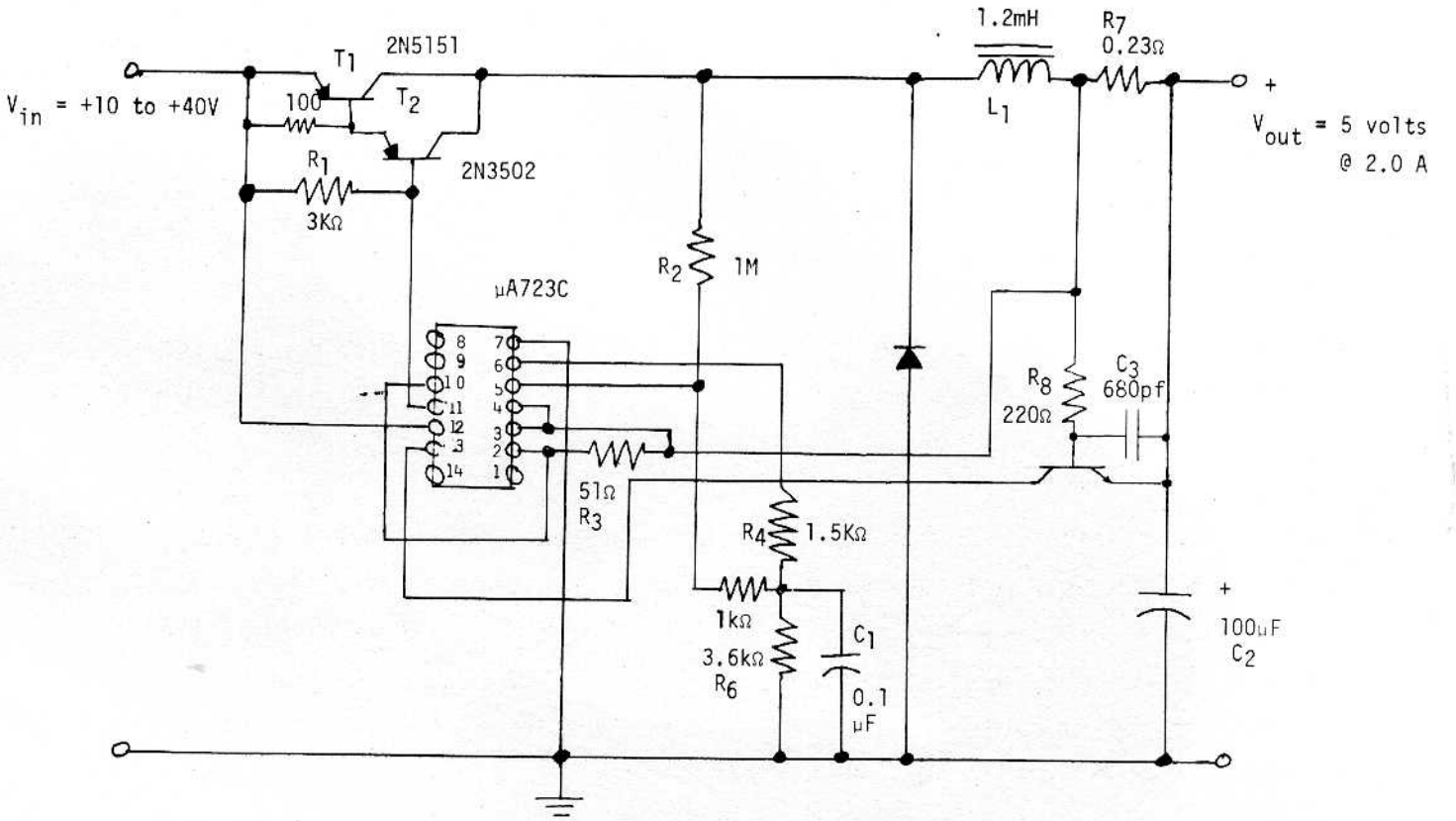


FIGURE 7: Positive Switching Regulator with Current Limiting